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Desenvolvimento de Circuitos de Ótica Integrada – Transrecetor Universal para NG-PON2

Photonic Integrated Circuits development – A Universal Transceiver for NG-PON2

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Dissertação apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Mestre em Engenharia Electrónica e Telecomunicações, realizada sob a orientação científica do Doutor António Luís Jesus Teixeira e do Doutor Mário José Neves de Lima, Professores do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro

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Palavras-chave Comunicações Óticas, NG-PON2, Chip, PIC, Transrecetor, Universal

Resumo

Nos últimos anos tem existido uma evidente evolução no mundo das telecomunicações, que vai desde novos serviços que requerem maiores velocidades e maior largura de banda, a um role de interações entre pessoas e máquinas, designada por *Internet of Things (IoT)*. Assim, a única tecnologia capaz de acompanhar este crescimento são as comunicações óticas.

Atualmente a solução que permite colmatar as necessidades do dia-a-dia, tais como trabalhar colaborativamente, comunicar por áudio e vídeo, e partilhar ficheiros, é baseada no *Gigabit-capable Passive Optical Network (G-PON)* com a mais recente evolução designada por *Next Generation Passive Optical Network Phase 2 (NG-PON2)*. Esta tecnologia baseia-se na multiplexagem no domínio do comprimento de onda e devido às suas características e desempenho torna-se a tecnologia mais vantajosa.

Um dos principais focos das comunicações óticas são os *Photonic Integrated Circuits (PICs)*. Estes conseguem englobar num único dispositivo vários componentes, o que simplifica o desenho do sistema ótico, reduzindo o espaço e o consumo de energia e melhora a confiabilidade. Estas caracteristicas tornam este tipo de dispositivos vantajosos para uma série de aplicações, justificando os investimentos no desenvolvimento da tecnologia para um nível muito elevado de desempenho e fiabilidade ao nível dos blocos de construção.

Com o objetivo de desenvolver as redes ópticas passivas de futuras gerações, este trabalho apresenta o desenho e a implementação de um PIC que visa ser um transrecetor universal para aplicações para NG-PON2. O mesmo PIC pode ser usado como *Optical Line Terminal (OLT)* ou como *Optical Network Unit (ONU)* e em ambos os casos como transmissor e recetor. Inicialmente é feito um estudo das redes óticas passivas e os seus *standards*. Seguidamente é feita uma abordagem teórica que explora um pouco dos materiais usados no desenvolvimento e produção de um PIC, quais as fábricas existentes, focando na SMART Photonics e os componentes usados no desenvolvimento deste *chip*. Com vista à concetualização do projeto, diferentes arquiteturas são desenhadas e a parte da cavidade do *laser* é simulada usando o Aspic™. Partindo da análise das vantagens e desvantagens de cada uma delas, é escolhida a melhor para utilizar na implementação. De seguida, a arquitetura do transrecetor é simulada bloco a bloco através do VPItransmissionMaker™ e é demonstrado o seu princípio de funcionamento. Finalmente é apresentada a implementação do PIC.

Keywords Optical Communications, NG-PON2, Chip, PIC, Transceiver, Universal

Abstract

In the last years there has been a clear evolution in the world of telecommunications, which goes from new services that need higher speeds and higher bandwidth, until a role of interactions between people and machines, named by Internet of Things (IoT). So, the only technology able to follow this growth is the optical communications.

Currently the solution that enables to overcome the day-by-day needs, like collaborative job, audio and video communications and share of files is based on Gigabit-capable Passive Optical Network (G-PON) with the recently successor named Next Generation Passive Optical Network Phase 2 (NG-PON2). This technology is based on the multiplexing domain wavelength and due to its characteristics and performance becomes the more advantageous technology.

A major focus of optical communications are Photonic Integrated Circuits (PICs). These can include various components into a single device, which simplifies the design of the optical system, reducing space and power consumption, and improves reliability. These characteristics make this type of devices useful for several applications, that justifies the investments in the development of the technology into a very high level of performance and reliability in terms of the building blocks.

With the goal to develop the optical networks of future generations, this work presents the design and implementation of a PIC, which is intended to be a universal transceiver for applications for NG-PON2. The same PIC will be able to be used as an Optical Line Terminal (OLT) or an Optical Network Unit (ONU) and in both cases as transmitter and receiver. Initially a study is made of Passive Optical Network (PON) and its standards. Therefore it is done a theoretical overview that explores the materials used in the development and production of this PIC, which foundries are available, and focusing in SMART Photonics, the components used in the development of this chip. For the conceptualization of the project different architectures are designed and part of the laser cavity is simulated using Aspic™. Through the analysis of advantages and disadvantages of each one, it is chosen the best to be used in the implementation. Moreover, the architecture of the transceiver is simulated block by block through the VPItransmissionMaker™ and it is demonstrated its operating principle. Finally it is presented the PIC implementation.

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List of Acronyms

APD Avalanche Photodiode

AWG Arrayed Waveguide Grating

BER Bit Error Ratio

CB Conduction Band

CMOS Complementary Metal-Oxide-Semiconductor

CT Channel Termination

CW Continuous Wave

DRC Design Rule Check

EA Electro-Absorption

FP-SOA Fabry-Pérot SOA

FPR Free Propagation Region

FSAN Full Service Access Network

FSR Free Spectral Range

FTTH Fibre to The Home

G-PON Gigabit-capable Passive Optical Network

IC Integrated Circuit

IoT Internet of Things

LPCVD Low-Pressure Chemical Vapor Deposition

MESFET Metal Semiconductor Field Effect Transistors

MMI Multi-Mode Interference

MMIR Multi-Mode Interference Reflector

MPA Mode Propagation Analysis

MPW Multi-project Wafer

MSM Metal Semiconductor-metal

MZM Mach-Zehnder Modulator

NG-PON2 Next Generation Passive Optical Network Phase 2

ODN Optical Distribution Network

OLT Optical Line Terminal

ONU Optical Network Unit

PDK Process Design Kit

PHASAR Phased Array

PIC Photonic Integrated Circuit

PM Phase Modulator

PON Passive Optical Network

PtP WDM Point-to-Point Wavelength Divison Multiplexing

QPSK Quadrature Phase Shift Keying

SME Small and Medium Enterprise

SNR Signal-to-Noise Ratio

SOA Semiconductor Optical Amplifier

SSG Small Signal Gain

TW-SOA Travelling Wave SOA

TWDM Time Wavelength Division Multiplexing

VB Valence Band

WGR Waveguide Grating Router

WM Wavelength Multiplexer

Chapter 1

Introduction

1.1 Overview

Nowadays, telecommunications play a key role in our daily lives, not only because the significance they have in allowing interaction between all of us, but also the forthcoming expansion of communication between machines, the so-called Internet of Things (IoT), which will result in the interconnection of thousands of millions of devices around the world. This huge growth of the Internet keeps a constant evolution of the telecommunications industry as it continues to be required increasingly greater bandwidth and faster speeds, thus challenging the limits of the capacity of the network [1].

Currently, the only communication technology to provide greater bandwidth to customers is optical communications because its transmission capacity is much higher compared to the previously existing copper systems. Thus, it arises the Passive Optical Networks (PONs). The PONs have a set of characteristics that make them a key element in the telecommunications industry, as they provide higher data rates, reduced power consumption and require less space in the core.

The PON technology used extensively by the telecommunications operators is the Gigabit-capable Passive Optical Network (G-PON). In order to develop the next generation, it has been explored the new standard, the Next Generation Passive Optical Network Phase 2 (NG-PON2). Defined for NG-PON2 is the capacity to transmit 40 Gbit/s in Downstream direction and 10 Gbit/s in Upstream direction [2]. Its appearance on the market is imminent and it is already being tested by a US telecommunications operator [3].

One can conclude that the complexity of the optical networks is increasing and for that a massive deployment of this technology inexpensive devices are needed. Thus, in order to keep up with the increased speed while keeping power consumption as low as possible Photonic Integrated Circuits (PICs) are utilized. PICs integrate optical elements on a small scale, such as lasers, modulators, optical amplifiers and multiplexers. These are the evolution in the optical domain, such as Integrated Circuits (ICs) are for electronics [4].

This dissertation aims to implement a PIC for NG-PON2 applications. This PIC is intended to be a universal transceiver. The same PIC will be able to be used as an Optical Line Terminal (OLT) or an Optical Network Unit (ONU) and in both cases as transmitter and receiver.

1.2 Motivation

In order to implement the latest generation of optical communications, the NG-PON2 technology, different solutions have been developed in order to be able to meet the defined specifications in terms of speed and compatibility.

In the existing Passive Optical Networks (PONs), such networks wherein the NG-PON2 is supported, two devices that determine the possible data rates to be transmitted are the OLT and the ONU. In these devices signals can be transferred in two directions, named Downstream and Upstream. For these two types of transmission, new transmitters and receivers need to be investigated to support such high transmission rates. These transmitters and receivers have optical modulation and demodulation as functioning base, that is achieved through electro-optical conversions [2].

These optical devices are implemented using PICs that can include in a single device several tens of optical components, capable of controlling the basic properties of light: amplitude, phase and polarization. However, in the provided speed gain by the closeness of the components and consequent minimization of the space occupied, one evident disadvantage is the increase in terms of the implementation cost. Another disadvantage is that when is needed implementation of different chips, there is an additional difficulty in the system aggregation due to the complexity of the packaging [4].

One possible evolution that could be developed would be a way to allow reduction of the number of chips necessary for NG-PON2 implementation. One of the difficulties in getting to integrate several functionalities in one chip is the required area occupied by filters and multiplexers. The multiplexers are essential to produce different transmission wavelengths for channel multiplexing, and the wavelengths of these channels vary depending on the direction of transmission. For this reason, developed chips for OLT are not directly compatible with the ones developed for ONU and vice versa.

In this dissertation it was developed one PIC that features a solution to successfully support multiple channels in a most generic way and using the fewest number of filters. In addition, most of the building blocks implemented on the chip work as bi-directional, so the chip can support both ways of transmitted signals also using less area as possible, featuring a unique optical interface for input and output.

1.3 Objetives

The main goals defined for the formulation of this dissertation are:

- Study the concepts about optical communications, such as the PON architectures, specifically the NG-PON2 standard;
- Present the advantages of PIC development and explore some design recommendations using the foundry manual;
- Specify the transceiver architecture to be used;
- Design of the PIC building blocks using simulation software;
- Simulate the complete solutions of the transmitter and receiver;
- Implement the layout of the developed PIC.

1.4 Structure

Apart of this introductory chapter, this dissertation is organized in more four chapters:

Chapter 2 - Optical Communications Standards and Integrated Photonics explores important concepts about optical communications for the development of this dissertation. Initially, it gives an approach to the NG-PON2 standard, following a description about PICs which includes references to the foundry design manual and theory about the building blocks.

Chapter 3 - Development of the Transceiver Architecture presents several proposals for the transceiver design including simulations and remarks of each one. The chapter finishes with the final architecture to be implemented.

Chapter 4 - Design and Simulation of the Transceiver describes the whole transceiver design procedure. It starts with the simulation of the filters that are part of the laser cavity using Aspic™. Then, each building block is simulated in VPItransmissionMaker™. Moreover, it is built a complete simulation for the transmitter and the receiver in VPItransmissionMaker™. Finally, it is shown the implementation of the PIC layout designed in OptoDesginer.

Chapter 5 - Conclusions and Future Work gives an overview of the dissertation, concludes the work done based on the objectives initially defined and suggests future work in order to improve the developed PIC.

1.5 Contributions

The main contributions of this work are:

- Description of the characteristics of Passive Optical Network (PON) standards, as well as the requirements for the implementation of a transceiver for NG-PON2;
- Analysis of the main characteristics and functional principles of the PIC building blocks;
- Introduction and discussion of several optical transceiver architectures;
- Development of an architecture for a universal transceiver for NG-PON2, using breakthrough solutions like the integration of an Arrayed Waveguide Grating (AWG) 4x2;
- Demonstration of the PIC functionality through simulations with the transceiver in transmitter and receiver modes;
- Design of the photonic integrated universal transceiver for NG-PON2.

Chapter 2

Optical Communications Standards and Integrated Photonics

Over the past few years, a major topic of concern for telecommunications operators has been the increase of the bandwidth used by the end user. This increase is due to the enormous growth of data, audio and especially video consumption. Also with the largest number of users, metropolitan area networks have been developed on a large scale, requiring research of latest generation infrastructures.

In this chapter, important concepts will be presented about optical communications for the development of the transceiver. Firstly, optical networks standards will be described, with major focus on NG-PON2. The chapter will conclude with a description about PICs which includes references to the foundry design manual and theory about the building blocks.

2.1 PON Architecture

In order to support the highly usage of bandwidth, optical communications networks that support high data rates had to be developed. Currently, the optical communications architectures in use are predominantly based on Passive Optical Networks (PONs).

A PON architecture is a system that combines network elements based in access optical networks of the type Optical Distribution Network (ODN). ODN is a point-to-multipoint optical fiber infrastructure that can be defined in two types [5]:

- **Simple ODN**: is composed entirely by passive elements and is represented by a single-rooted point-to-multipoint tree of optical fibres with splitters, combiners and filters.
- **Composite ODN**: consists of two or more simple ODNs interconnected by active devices.

Figure 2.1 illustrates an example of a PON architecture. In this example, not only is possible to observe each one of the ODN types, but also the coexistence of them in a single PON network. At the ends of the PON networks, there are two types of devices that translate the optical signals. These are fundamental components in the PON architecture and are named as Optical Line Terminal (OLT) and Optical Network Unit (ONU). They are defined by the following [5]:

- **OLT:** is the device located in the telecommunications operator terminal and it has the function to transmit and receive data to and from several users.
- **ONU:** is the device that terminates the network in the user side.

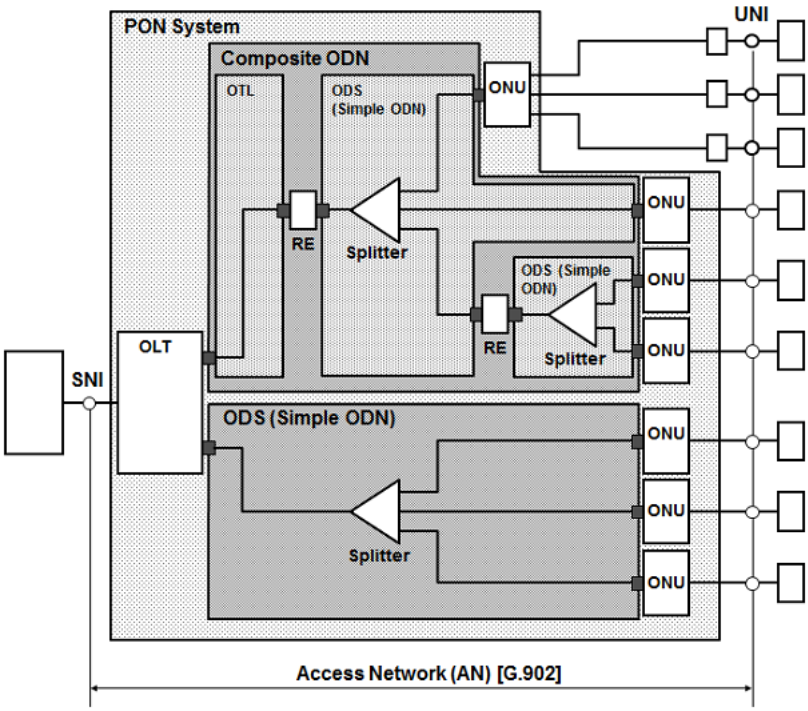


Figure 2.1: Example of a PON architecture [5].

On the communication between these two devices, multiple channels are used in order to transmit high data rates and at the same time it is also necessary to transmit simultaneously to several users. This occurs in two transmission directions in each ODN, which are defined as [5]:

- **Downstream**: is the direction which the signals are transmitted from the OLT to the ONU. In this case, the OLT is the transmitter and the ONU is the receiver.
- **Upstream**: is the direction which the signals are transmitted from the ONU to the OLT. In this case, the OLT is the receiver and the ONU is the transmitter.

In both directions of the transmission, Downstream and Upstream, the same components and optical fibers are used. This type of configuration is designated as duplex [5].

2.2 NG-PON2 Standard

Next Generation Passive Optical Network Phase 2 (NG-PON2) is defined as a PON system with a nominal aggregate capacity of 40 Gbit/s in the Downstream direction and 10 Gbit/s in the Upstream direction [5]. This technology is implemented based in a suite of protocols specified in the ITU-T G.989.x series Recommendations, specifically in G.989.2 standard.

A NG-PON2 system is composed by a set of Time Wavelength Division Multiplexing (TWDM) channels and/or by a set of Point-to-Point Wavelength Divison Multiplexing (PtP WDM) channels. The main focus of the PON systems is in the TWDM type, as it was considered by the Full Service Access Network (FSAN) a solution that in the operators point of view it is considered less risky, less disruptive and less expensive compared to other solutions. Thus, the usage of PtP WDM technologies is optional.

In a PON system with multiple channels, which is the case of the NG-PON2, the OLT is frequently composed by multiple Channel Terminations (CTs) connected by a Wavelength Multiplexer (WM) [5]. This allows simultaneously data transmission in several channels that makes possible to attend quickly each one of the ONUs. The reference model of the NG-PON2 is presented in Figure 2.2, where it can be observed a scheme of this topology.

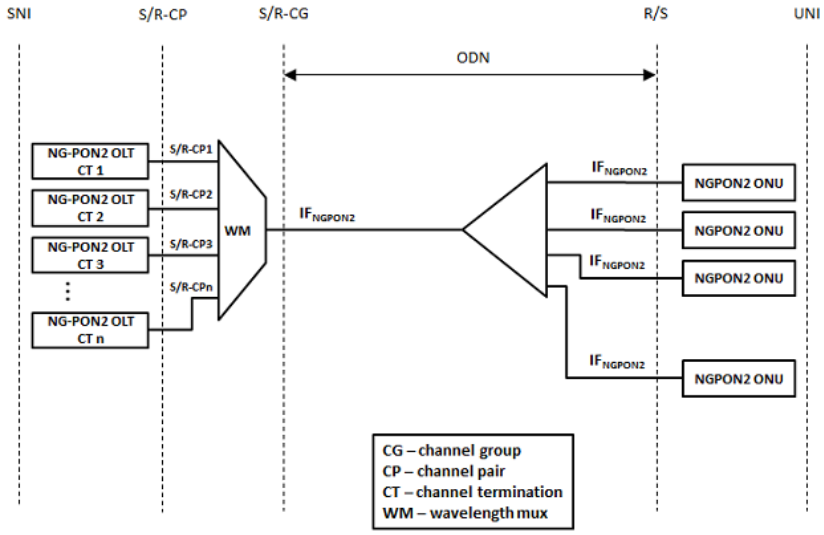


Figure 2.2: Reference model of the NG-PON2 [5].

Each ONU has a transmitter and a receiver which are adjustable. The transmitter is set to the allocated channel in the Upstream of the TWDM. Likewise, the receiver is tuned to the allocated channel in the Downstream of the TWDM. Based on the standard, it is specified that the system has to have a minimum of four channels of the TWDM, which can be extended to a total of eight channels [5].

The NG-PON2 wavelength plan has been defined to enable the coexistence through wavelength overlay with legacy PON systems, for example the Gigabit-capable Passive Optical Network (G-PON). Thus, the wavelength range defined in the TWDM for the Downstream is from 1596 nm to 1603 nm. In case of the Upstream, it is defined in three types: Wide Range (1524-1544 nm), Reduced Range (1528-1540 nm) and Narrow Range (1532-1540 nm) [5].

It was defined for NG-PON2 two different speed transmissions: 2.48832 Gbit/s and 9.95328 Gbit/s. The following tables, Table 2.1 and Table 2.2, summarize some specified parameters for the transmitter of the OLT, for 2.48832 Gbit/s transmission and for 9.95328 Gbit/s transmission respectively [5].

Table 2.1: Optical Interface Parameters of the transmitter in Downstream for 2.48832 Gbit/s

Nominal line rate	2.48832 Gbit/s			
Operating channel spacing	100 GHz			
Line code	Scrambled NRZ			
Minimum side mode suppression ratio	30 dB			
ODN Class	N1	N2	E1	E2
Mean channel launch power MIN	+0.0 dBm	+2.0 dBm	+4.0 dBm	+6.0 dBm
Mean channel launch power MAX	+4.0 dBm	+6.0 dBm	+8.0 dBm	+10.0 dBm

Table 2.2: Optical Interface Parameters of the transmitter in Downstream for 9.95328 Gbit/s

Nominal line rate	9.95328 Gbit/s			
Operating channel spacing	100 GHz			
Line code	Scrambled NRZ			
Minimum side mode suppression ratio	30 dB			
ODN Class	N1	N2	E1	E2
Mean channel launch power MIN	+3.0 dBm	+5.0 dBm	+7.0 dBm	+9.0 dBm
Mean channel launch power MAX	+7.0 dBm	+9.0 dBm	+11.0 dBm	+11.0 dBm

Table 2.3 and Table 2.4 summarize some specified parameters for the receiver of the ONU, for 2.48832 Gbit/s transmission and for 9.95328 Gbit/s transmission respectively [5]. These parameters are mainly related to the Bit Error Ratio (BER).

Table 2.3: Optical Interface Parameters of the receiver in Downstream for 2.48832 Gbit/s

BER	10^{-4}
Sensitivity at BER reference level	-30.0 dBm
Overload at BER reference level	-10.0 dBm

Table 2.4: Optical Interface Parameters of the receiver in Downstream for 9.95328 Gbit/s

BER	10^{-3}
Sensitivity at BER reference level	-28.0 dBm
Overload at BER reference level	-7.0 dBm

The TWDM channels Downstream frequency plan is shown in Table 2.5 [5].

Table 2.5: TWDM Channel Downstream Frequency Plan

Channel	Frequency (THz)	Wavelength (nm)
1	187.8	1596.34
2	187.7	1597.19
3	187.6	1598.04
4	187.5	1598.89
5	187.4	1599.75
6	187.3	1600.60
7	187.2	1601.46
8	187.1	1602.31

For the Upstream, the opposite direction of transmission, some specified parameters are also summarized in Tables 2.6 and 2.7 for the transmitter of the ONU. Firstly for the 2.48832 Gbit/s transmission and then for the 9.95328 Gbit/s transmission [5].

Table 2.6: Optical Interface Parameters of the transmitter in Upstream for 2.48832 Gbit/s

Nominal line rate	2.48832 Gbit/s	
Minimum Operating channel spacing	50 GHz	
Maximum Operating channel spacing	200 GHz	
Line code	Scrambled NRZ	
Minimum side mode suppression ratio	30 dB	
	Type A	Type B
Mean channel launch power MIN	+4.0 dBm	+0.0 dBm
Mean channel launch power MAX	+9.0 dBm	+5.0 dBm

Table 2.7: Optical Interface Parameters of the transmitter in Upstream for 9.95328 Gbit/s

Nominal line rate	9.95328 Gbit/s	
Minimum Operating channel spacing	50 GHz	
Maximum Operating channel spacing	200 GHz	
Minimum side mode suppression ratio	30 dB	
	Type A	Type B
Line code	Scrambled NRZ (20 km)	FFS (40 km)
Mean channel launch power MIN	+4.0 dBm	+2.0 dBm
Mean channel launch power MAX	+9.0 dBm	+7.0 dBm

Table 2.8 and Table 2.9 summarize some specified parameters for the receiver of the OLT, for 2.48832 Gbit/s transmission and for 9.95328 Gbit/s transmission respectively [5].

Table 2.8: Optical Interface Parameters of the receiver in Upstream for 2.48832 Gbit/s

BER	10^{-4}			
Sensitivity at BER reference level	N1	N2	E1	E2
Type A	-26.0 dBm	-28.0 dBm	-30.5 dBm	-32.5 dBm
Type B	-30.0 dBm	-32.0 dBm	-34.5 dBm	-36.5 dBm
Overload at BER reference level	N1	N2	E1	E2
Type A	-5.0 dBm	-7.0 dBm	-9.0 dBm	-11.0 dBm
Type B	-9.0 dBm	-11.0 dBm	-13.0 dBm	-15.0 dBm

Table 2.9: Optical Interface Parameters of the receiver in Upstream for 9.95328 Gbit/s

BER	10^{-3}			
Sensitivity at BER reference level	N1	N2	E1	E2
Type A	-26.5 dBm	-28.5 dBm	-31.0 dBm	NA
Type B	-28.5 dBm	-30.5 dBm	-33.0 dBm	-33.0 dBm
Overload at BER reference level	N1	N2	E1	E2
Type A	-5.0 dBm	-7.0 dBm	-9.0 dBm	NA
Type B	-7.0 dBm	-9.0 dBm	-11.0 dBm	-11.0 dBm

The TWDM channels Upstream frequency plan is shown in Table 2.10 [5].

Table 2.10: TWDM Channel Upstream Frequency Plan

Channel	Frequency (THz)	Wavelength (nm)
1	195.6	1532.68
2	195.5	1533.47
3	195.4	1534.25
4	195.3	1535.04
5	195.2	1535.82
6	195.1	1536.61
7	195.0	1537.40
8	194.9	1538.19

2.3 Photonic Integrated Circuits (PICs)

For the past years there has been a clear evolution in the implementation and development of the optical fiber distribution. Optical fiber is now connecting not only servers and main nodes but also houses. This implementation is named Fibre to The Home (FTTH). This technology enables the offer of applications to a high flow rate per client. This evolution requires high transmission data rates and types of modulation with large spectral density, for example Quadrature Phase Shift Keying (QPSK) [6].

As the complexity of such optical networks is increasing, in terms of the optical hardware, currently, most of the components are discrete. In order to suit with the increased speed and to maintain the power consumption as low as possible, Photonic Integrated Circuits (PICs) must be implemented. PICs contain optical elements in a very small scale, like optical amplifiers and optical multiplexers. They are the evolution for the optical domain, as the electronic Integrated Circuits (ICs) are for electronic [7].

PICs are able to control several light properties as amplitude, phase and polarity. The usage of PICs is also a good advancement in terms of the design of the optical system, since the required space and the power consumption are reduced. At the same time, as the system is more integrated, reliability is also improved [7].

2.3.1 Materials and Foundries

An important evolution in progression is the cost reduction by developing different products in a single or a few highly standardized processes. So, a generic foundry model for photonics is needed. For instance, in silicon microelectronics a number of chip manufacturers are providing foundry access.

InP-based generic photonic integration technology has been explored in a number of European projects. Access to InP-based generic foundry processes is now organized by the JePPIX platform, in which Europe's key players in the field of InP-based photonic integration technology are cooperating [4].

Nowadays, three chip manufacturers offer access to InP-based generic foundry processes: Oclaro - United Kingdom, the Fraunhofer Heinrich Hertz Institut - Germany and SMART Photonics - the Netherlands [4].

A few cleanroom owners provide access to fabless customers in order to share the burden of the cleanroom operational expenditure. In this way, a fabless customer can avoid the huge investment in a fab and restrict investment just to the development costs of a specific integration process for a specific PIC. Still, significant volumes and the investment costs are needed and, in combination with risk, it turns to be prohibitive for most Small and Medium Enterprises (SMEs).

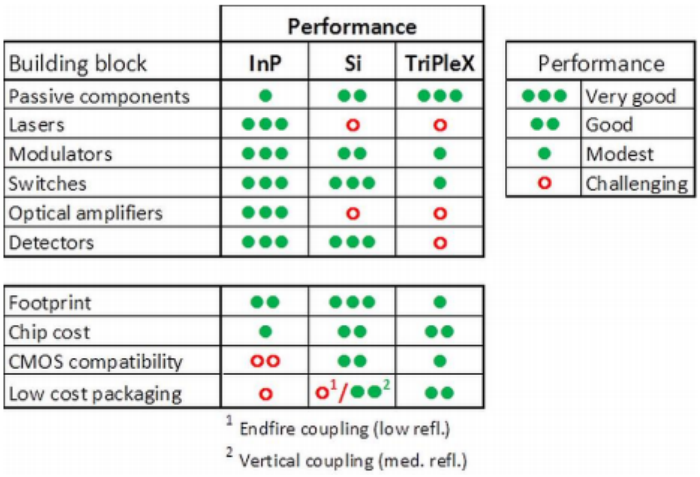
A dramatic further cost reduction can be achieved if the chip design is based on a standardized integration process where the development costs can be shared by many users. Then, the entry costs are mainly restricted to design costs. The design costs can be reduced even further by developing dedicated Process Design Kits (PDKs) with component libraries that contain the mask layout and accurate models of the building blocks in the foundry platform. It will make entry costs for development of PICs affordable for most SMEs. Moreover, it is expected that the introduction of the generic model by JePPIX platform will lead to a rapid expansion in the application of PICs [4].

Apart from InP-based foundries there is another platform named ePIXfab. ePIXfab is the photonics alliance with silicon processes. Some of them are: CEA-LETI, imec, VTT and IHP. Working with silicon-based PICs have several advantages as lower cost solution and, in the near future, the possibility of monolithic electronics integration. Although, some key blocks are still not available and they face serious challenge of development: lasers and optical amplifiers.

A third platform is TriPleX™, a technology owned and developed by LioniX – the Netherlands. In this technology, the waveguides are based on Low-Pressure Chemical Vapor Deposition (LPCVD) processing of alternating Si3N4 and SiO2 layers. It is also a low-cost

solution and integrates Complementary Metal-Oxide-Semiconductor (CMOS) - compatible fabrication equipment [4].

A summarized table is presented in Figure 2.3, where it is possible to compare different parameters and blocks availability among the different platforms explained before.



	Performance		
Building block	InP	Si	TriPleX
Passive components	●	●●	●●●
Lasers	●●●	o	o
Modulators	●●●	●●	●
Switches	●●●	●●●	●
Optical amplifiers	●●●	o	o
Detectors	●●●	●●●	o
Footprint	●●	●●●	●
Chip cost	●	●●	●●
CMOS compatibility	oo	●●	●
Low cost packaging	o	o[1]/●●[2]	●●

Performance	
●●●	Very good
●●	Good
●	Modest
o	Challenging

[1] Endfire coupling (low refl.)
[2] Vertical coupling (med. refl.)

Figure 2.3: Table of comparison of different parameters and blocks among different technologies [8].

2.3.2 SMART Photonics

SMART Photonics is a pure-play foundry, it means that they do not produce their own products. It is located in Eindhoven, Netherlands. SMART Photonics in collaboration with the COBRA research institute offers a generic integration process development, which allows fast prototyping and low cost development without compromising performance and functionality. Their work is essential based in InP processing with a broad experience in applications like telecommunications, medical, sensing and much more [9].

Custom designed PICs can be developed using the SMART Photonics Process Design Kit (PDK). This PDK consists of an extensive building block library and design rules. This standardization is based on a design method which enables to freely combine a limited number of photonic building blocks to form complex photonic circuits. A Design Manual of the PDK is available, that has the objective of describing the building blocks, their characteristics and geometric constraints imposed by the process. Each building block description contains relevant information to the software design tool. Moreover, it describes some additional items such as the metal routing and the finishing of the chips.

2.3.2.1 Design Flow

The development process of a PIC can be divided into several stages, which form a design flow. To begin the project development some minimum requirements are necessary, as the information about the components available and compatible software with the foundry libraries to simulate and to do the layout design [10].

The design flow can be described in the following steps:

1. Develop an architecture that implements the desired application, based on appropriate and available components.
2. Study the building blocks available in the Design Manual.
3. Implement the circuit in the software simulation.
4. Compare the simulation results with the desired specifications.
5. Select one of the predefined cells in the wafer that best suits the required specifications.
6. Design the layout of the circuit with the selected building blocks.
7. Make sure that the layout follows the manual rules by running the Design Rule Check (DRC) tests.
8. Send the GDSII file type to the foundry, which will also double-check the design through the DRC tests and tile the design into the Multi-project Wafer (MPW).
9. Receive the die from the foundry to perform laboratory tests and/or send to the packaging.

2.3.2.2 Platform Process Description

In order to be succeed in the development process of a PIC, it is essential to follow properly the rules of the foundry. A first step would be to have important knowledge of the layerstack. Figure 2.4 shows the layerstack of the SMART Photonics active and passive wafers.

For a short explanation, the red color indicates the active layer, green is the waveguiding film and blue the cladding layer. The roman numerals indicate the different epitaxial growth.

Active

Layer	Material	Thickness
III-2	p-InGaAs	>1500nm
III-1	p-InP	
I-5	p-InP	
I-4	i-Q1.25	
I-3	i-MQW	500nm
I-2	i-Q1.25	
I-1	n-InP	
I-0	n-InP	substrate

Passive

Layer	Material	Thickness
III-2	p-InGaAs	>1500nm
III-1	p-InP	
II-2	n-InP	
II-1	n-Q1.25	500nm
I-1	n-InP	
I-0	n-InP	substrate

Figure 2.4: SMART active-passive layer stack. The active layer (red) consists of multiple quantum wells [10].

Figure 2.5 presents an overview of used complex refractive indices of some materials. The values listed are for a 1.55 μm wavelength and they are important for modeling the waveguides. It is important to know that it is not necessary to include all the details about this layer stack, because best results are achieved when using a simple structure in the simulation.

Now it will be explored the predefined active regions. There are predefined cells with a fixed size and location on the wafer for the SMART Photonics MPW, as one can see in Figure 2.6.

material	doping [cm^{-3}]	α [dB/cm]	α [cm^{-1}]	n'	n''
Au				0.18	-10.2
Pt				5.31	-7.04
Ti				3.70	-4.5
p-InGaAs	$1 \cdot 10^{19}$			3.7434	-0.287
p-InP	$1 \cdot 10^{18}$	99	22.80	3.1645	$-2.81 \cdot 10^{-4}$
p-InP	$5 \cdot 10^{17}$	49.5	11.40	3.1669	$-1.41 \cdot 10^{-4}$
p-InP	$3 \cdot 10^{17}$	29.7	6.84	3.1693	$-8.44 \cdot 10^{-5}$
p-Q1.25	$1 \cdot 10^{17}$	9.9	2.28	3.3634	$-2.81 \cdot 10^{-5}$
p-Q1.25	n.i.d.	0	0	3.3640	0
n-Q1.25	$6 \cdot 10^{16}$	0.26	0.06	3.3636	$-7.40 \cdot 10^{-7}$
n-Q1.3	$6 \cdot 10^{16}$	0.26	0.06	3.3892	$-7.40 \cdot 10^{-7}$
n-InP	$3.5 \cdot 10^{17}$	1.52	0.35	3.1676	$-4.32 \cdot 10^{-6}$
n-InP	$5 \cdot 10^{17}$	2.17	0.5	3.1669	$-6.17 \cdot 10^{-6}$
n-InP	$1 \cdot 10^{18}$	4.34	1	3.1645	$-1.23 \cdot 10^{-5}$

Figure 2.5: Overview of used complex refractive indices [10].

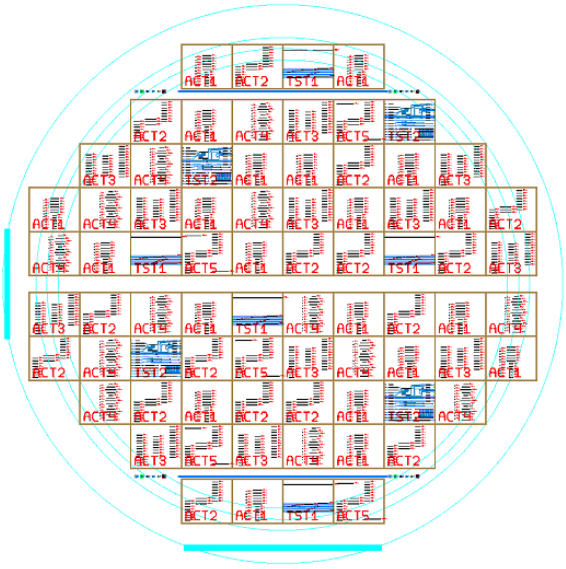


Figure 2.6: Layout of the different cells on a 2 inches wafer [10].

A total of 76 cells can be accomodated on a 2 inches wafer, however only 64 are available to users. There are five different user design cells and two different test cells in the COBRA MPW, that are labeled "ACT1"–"ACT5" and "TST1"–"TST2" respectively. The difference between them is the distance from the wafer edge. If cells are 5 mm or closer to the wafer edge, cells are available, otherwise they are considered usable only for testing. All cells measure 4.6 x 4.0 mm^2. An example of a cell layout is shown in Figure 2.7 [10].

The vertical direction of each cell is the cleave direction. The cleaving ensures a flat surface almost perfect as end-point for the access waveguides to the circuit. In the horizontal direction, the quality is not as good, and no waveguides should end on those chip edges [10].

Figure 2.7: Example of a cell layout [10].

2.4 Photonic Integrated Circuit Components

With the development of PICs, one focal point is the concern about the choice of appropriate components for integration. There is a very wide range of components, each one with a specific function. However, there is a constant research on the components for integrated photonics with the aim to improve their characteristics and discover new applications. These components have a wide range of trade-offs between performance, technology maturity and structural compatibility [4].

In this section it will be done a brief explanation in terms of the main performance features about the components that will be used in the development of the transceiver.

2.4.1 Arrayed Waveguide Grating (AWG)

Arrayed Waveguide Grating (AWG), also known as Phased Array (PHASAR) and Waveguide Grating Router (WGR), is an optical planar passive device that can be used as multiplexer and as demultiplexer. It is based on an array of waveguides with both imaging and dispersive properties. Basically the image of the field at the input waveguide has the same field at the output waveguide, but in a dispersive way. This means that the different wavelength signals present in the input waveguide are imaged onto different output waveguides [11].

AWGs have been in development through the past years. Nowadays they can operate in a long wavelength window and can have N inputs for N outputs, known by wavelength routers, instead of having only one input for N outputs. AWGs are the most important filter type applied in multi-wavelength network applications. However, they can be used in other areas such as signal processing, measurement, characterization and sensing [12].

Using AWGs have several advantages, for example: compactness, fabrication stability, reliability, reduced cost of fabrication and packaging and high precision on the control of channel spacing (in compliance with the ITU-T).

The schematic layout of an AWG-demultiplexer is shown in Figure 2.8, as one can see, the light input is propagated through the transmitter waveguide, enters the first Free Propagation Region (FPR) that is no longer laterally confined and gets diffracted. On arriving at the input aperture the light gets coupled into the waveguide array structure that is propagated through the individual waveguides in direction to the output aperture.

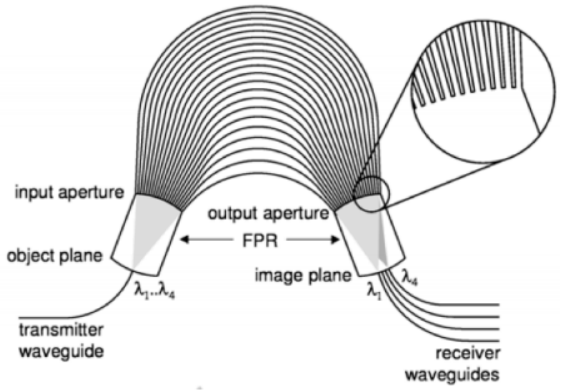


Figure 2.8: Geometry of an AWG-demultiplexer [11].

The length of each individual waveguide of the array is determined by the optical path length difference between adjacent waveguides and it is equal to an integer multiple of the central wavelength (λ_c) of the demultiplexer. The fields in the individual waveguides arrive at the output with the same phase for the central wavelength (λ_c), and thus the divergent beam at the input aperture is reproduced at a convergent one at the output with the same amplitude and phase distribution.

The spatial separation of different wavelengths is due to the linear increase of the length of the array waveguides, which introduces a wavelength-dependent tilt of outgoing beam and the focal point shifts along the image plane. If receiver waveguides are located at appropriate positions along the image plane, different wavelengths are led to different output ports. Figure 2.9 shows the input field at the object plane will be formed in the center of the image plane [11].

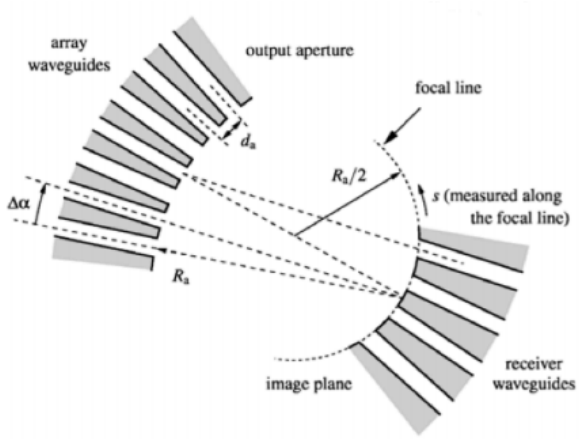


Figure 2.9: Beam focusing geometry in the free propagation region [11].

The length difference between adjacent array waveguides enables focusing of the fields propagating in an AWG. This length difference is given by:

$$\Delta L = m.\frac{\lambda_c}{\eta_{eff}} \tag{2.1}$$

Where m is called the order of the phased array, λ_c is the central wavelength and η_{eff} is the effective refractive index of the waveguide mode and λ_c/η_{eff} corresponds to the wavelength inside the array waveguides. Due to this, the array acts as a lens with image and object planes at a defined distance of the array apertures, R_a. This geometry, shown in Figure 2.9, represents a Rowland-type mounting where the receiver and transmitter waveguides should be located along a circle with radius half of R_a [11].

The length increment ΔL of the array provides an increase to a phase difference giving by:

$$\Delta\phi = \beta\Delta L \tag{2.2}$$

where β is the propagation constant in the waveguides and is written by:

$$\beta = \frac{2\pi\nu\eta_{eff}}{c} \tag{2.3}$$

considering ν as the frequency of the propagating wave and c as the speed of light in vacuum. The spatial dispersion of the AWG is represented by the lateral displacement of the focal spot along the image plane per unit frequency that is defined by:

$$D_{sp} = \frac{1}{\nu c}\frac{\eta_g}{\eta_{FPR}}\frac{\Delta L}{\Delta\alpha} \tag{2.4}$$

with η_{FPR} the mode index in the FPR, $\Delta\alpha$ the divergent angle between the array waveguides in the fan-in and the fan-out sections, and n_g the group index of the waveguide mode:

$$n_g = n_{eff} + \nu\frac{dn_{eff}}{d_v} \tag{2.5}$$

The spatial dispersion is fully determined by the order m and the divergence angle $\Delta\alpha$, and as a consequence filling-in of the space between the array waveguides close to the apertures due to finite lithographical resolution does not affect the dispersive properties of the AWG [11].

The response of the AWG is periodic, if the input wavelength change is such that the phase difference $\Delta\phi$ between adjacent waveguides has increased by 2π, the transfer will be the same as before. So the Free Spectral Range (FSR) is the period in frequency domain and can be written by:

$$FSR = \frac{\nu_c}{m}\left(\frac{\eta_{eff}}{\eta_g}\right) \tag{2.6}$$

Channel crosstalk is the contribution of undesirable signals that can be caused by several mechanisms, due to fabrication design imperfections and it is an important characteristic in AWGs. The maximum crosstalk value measured with one active input channel is a common measurement usually referred as single-channel crosstalk level [12].

There are several mechanisms that cause crosstalk: receiver crosstalk, truncation, mode conversion and coupling in the array. The last two are caused mainly by the fabrication [12].

Receiver crosstalk represents the coupling between the receivers due to the tails of the field distributions. In an ideal case the field would not be truncated but as in the AWG the array aperture is finite, so truncation causes crosstalk. In mode conversion, "ghost" images

can appear due to the excitation of the first order modes in the junctions between straight and curved waveguides, if the waveguides are not strictly single mode. The coupling in the array is induced due to the coupling in the input and output sections in the arrays [12].

2.4.2 Multi-Mode Interference (MMI) Devices

Multi-Mode Interference (MMI) devices are integrated optic components that use the self-imaging principle. This principle was first studied more than 150 years ago and it was stated by Lucas B. Soldano and Erik C.M. Pennings as: "Self-imaging is a property of multimode waveguides by which an input field profile is reproduced in single or multiple images at periodic intervals along the propagation direction of the guide" [13].

A MMI device is composed by a multimode waveguide where the interference phenomena occur. At the extremes it has N inputs and M outputs access waveguides, which have a defined width and placement and are tapered to single mode waveguides. It can be used in a broad number of applications, making its integration in the design of PICs very usual. Examples of applications are: ring lasers, optical gates, optical couplers and optical switches. MMI devices have several advantages: reliability, fabrication easiness and robustness.

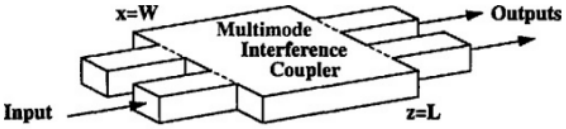


Figure 2.10: Multi-Mode Interference device diagram [14].

One way to describe the self-imaging phenomena in multimode waveguides is using the full-modal propagation analysis. For the formulation of the periodic imaging, the guided Mode Propagation Analysis (MPA) is followed. In order to understand where to find the desire images, using MPA, the field profile along the waveguide is written by [13]:

$$\psi(y, L) = \sum_{v=0}^{m-1} c_v \psi_v(y) e^{j \frac{v(v+2)\pi}{3L\pi} L} \tag{2.7}$$

where c_v is the field excitation coefficients, ψ_v the modal field distribution of mode v and L the length of the device.

The field $\psi(y, L)$ can be a reproduction (self-imaging) of the input field $\psi(y, 0)$. It is called General Interference to the self-imaging mechanisms which are independent of the modal excitation; and Restricted Interference to the mechanisms which are acquired by exciting certain modes alone.

The exponential term in the equation is called the mode phase factor. To obtain a single image, this factor has to be either 1 or $(-1)^v$. The first condition represents a direct replica of the input field and the second condition even modes will be in phase and the odd modes in anti-phase. Thus, in general interference, single images of the input field will appear at a distance even and odd multiple of $3L_\pi$. For multi-fold images, they are formed at intermediate positions. Based on mathematical analysis, N images are obtained at the distances:

$$L = \frac{p}{N}(3L_\pi) \tag{2.8}$$

with $p \geq 0$ and $N \geq 1$ which are integers with no common divisor.

The restricted interference is divided in two cases: paired and symmetric interference. For the first, each even mode leads its odd partner by a phase difference of $\frac{\pi}{2}$ at $z = \frac{L_\pi}{2}$. In the symmetric interference the image is acquired by linear combination of the even symmetric modes.

Table 2.11 summarizes the characteristics of the general and restricted (paired and symmetric) interferences [13].

Table 2.11: Summary of the characteristics of the general and restricted interferences

Interference mechanism	General	Paired	Symmetric
Inputs x Outputs	$N \times N$	$2 \times N$	$1 \times N$
First single image distance	$3L_\pi$	L_π	$(3L_\pi)/4$
First N-fold image distance	$(3L_\pi)/N$	$(L_\pi)/N$	$(3L_\pi)/(4N)$
Excitation requirements	none	$c_v = 0$ for $v = 2, 5, 8...$	$c_v = 0$ for $v = 1, 3, 5...$
Input(s) location(s)	any	$y = \pm W_e/6$	$y = 0$

2.4.3 Semiconductor Optical Amplifier (SOA)

Semiconductor Optical Amplifier (SOA) is an active optical component. It involves a dynamic interaction between light and matter and has an optical gain, which is caused by the recombination of electrons and holes that are injected by external current. Basically it works like a semiconductor laser, however with a higher current density than a laser at threshold.

The historical development of SOAs is truly related to the semiconductor lasers. The first studies started in the 1960s where the first devices were based on GaAs homojunctions operating at low temperatures. When the double heterostructure appeared, SOAs gain further improvements and at the time of 1980s most of the research was carried using InP/InGaAsP that operates in 1300 to 1600 nm. Until the end of 80s the devices had an asymmetric waveguide structure leading to strongly polarization sensitive gain, but in 1989 the first polarization insensitive was demonstrated. In 1990s was possible to have lower polarization dependence with a high gain, accompanied by high saturation power and high bandwidth. At this time SOAs have become commercially available [15].

The fundamental characteristics of SOAs technology: very compact device, low input power requirements, high gain, large optical bandwidth, very short response times, the fact they are cheap and the multi-functional applications including in optical switches, modulators, wavelength converters and in the integration with other active or passive optical components. With these characteristics the SOAs are increasingly becoming a high desirable PIC component.

The operation of a SOA requires a p-n double heterojunction, providing carrier confident and optical guiding. Figure 2.11 shows a schematic diagram of a SOA. The active region conveys gain to the input signal, where it is used an external current that gives enough energy to convert the state (and gain takes place again). To confine a propagating signal is used an embedded waveguide, however the optical confinement is weak and some of the signal will leak to the surrounding cladding regions. The output signal has additive noise, produced by the amplification process and cannot be fully avoided. The gain spectrum had also ripples that cannot be avoided, since they are introduced by amplifying facets that are reflective [15].

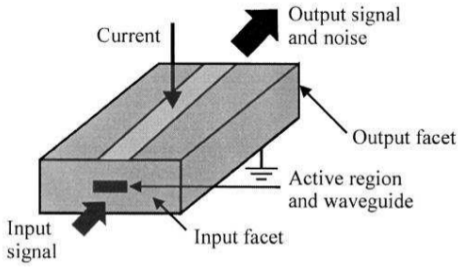
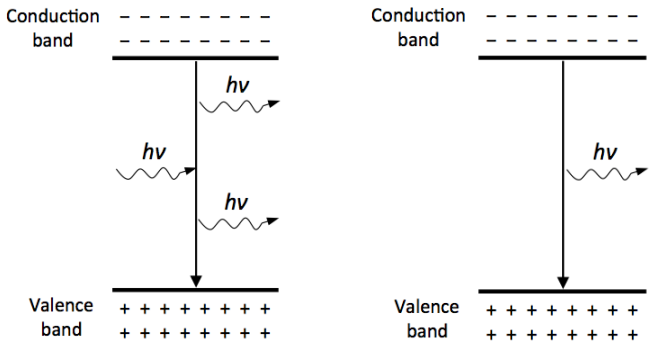


Figure 2.11: Schematic diagram of a SOA [15].

Applying an external current source, this will inject carriers in the active region of the SOA, the Conduction Band (CB). During this process, holes are left in the ground state, known as Valence Band (VB).

Three radioactive mechanisms may happen in the semiconductor: stimulated absorption, stimulated emission and spontaneous emission. In simulated absorption, an incident light photon of sufficient energy stimulates a carrier to the CB from the VB. The incident photon is then extinguished, so we can consider as a loss process. Stimulated emission (Figure 2.12) occurs with the recombination of a carrier in the CB with a hole in the VB. A photon is originated and it is identical to the incident photon. If it is applied enough injection current placing more population in the CB than in the VB, there is more stimulation than absorption, and the semiconductor will have optical gain. Finally, there is also the possibility of a photon to be emitted though spontaneous emission (Figure 2.12). In this case, a carrier in the CB is recombined with a hole in the VB, but in a spontaneously way. The new photon will have random frequency and phase, adding an undesirable effect as noise, and it will reduce the available carrier population to produce optical gain [15].



(a) Stimulated Emission. (b) Spontaneous Emission.

Figure 2.12: Stimulated and Spontaneous Emission.

SOAs can be distinguished in two types (Figure 2.13): Fabry-Pérot SOA (FP-SOA) and Travelling Wave SOA (TW-SOA). The main difference between them is related to the reflectivity's facets. In FP-SOA, the signal passes through the amplifier, so reflectivity's facets are significant and because of that it is known to be a resonant amplifier. Here, high gain can be obtained at low injection and usually implies operation at bias current just below the lasing threshold. However these devices are extremely dependent on the

polarization, wavelength of the signal, bias current and temperature and have low saturation power [15].

The TW-SOA is the opposite; the signal undergoes a single-pass of the amplifier because the end facets have applied antireflection coatings, which reduce the reflectivity. TW-SOA has higher spontaneous emission noise, however it features higher bandwidth, reduced polarization, temperature and current sensitivity and high saturation powers. Due to its proprieties, TW-SOA replaced FP-SOA in most of the applications [15].

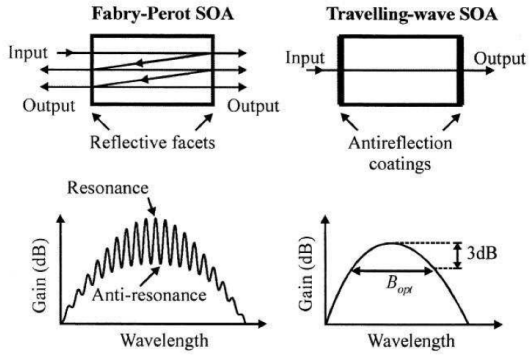


Figure 2.13: Basic types of SOA and associated gain spectrum [15].

Gain is one of the most important parameters of an optical amplifier and it is defined as the ratio between the optical power at the output and at the input. When the input power increases, the gain of any amplifier saturates (Figure 2.14). It is important to note that operating SOAs under saturation may cause pulse distortion. Another important parameter is the bandwidth. Small Signal Gain (SSG) is known to be the highest achievable gain. The bandwidth is defined when the gain is 3 dB lower than the peak SSG [16].

Figure 2.15 shows a typical gain spectrum for an implemented SOA from SMART photonics for different pump current densities. For larger current densities the gain increases until this improvement starts to saturate at a certain point. Moreover, it can be observed that the wavelength of the peak gain shifts for different currents.

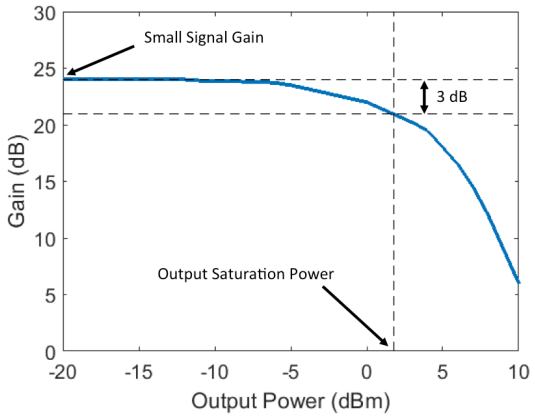


Figure 2.14: Gain over Output Power.

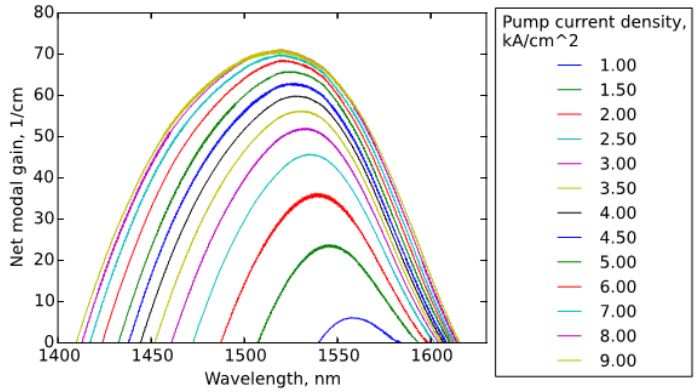


Figure 2.15: Gain over wavelength. The colors indicate the pump current density [10].

2.4.4 Mach-Zehnder Modulator (MZM)

There are two types of modulation, direct modulation and external modulation. Direct modulation works with the variation of the laser power that turns on and off according to the data signal. Using direct modulation leads to have several disadvantages for instance chirp in the output signal, inefficient usage of the spectrum and relatively low bit rates. All of these followed to the usage of the external modulation. External modulation uses an external modulator that modulates constant power coming from the laser. There are several types of external modulators, like Electro-Absorption (EA), Phase Modulator (PM) and Mach-Zehnder Modulator (MZM) [17].

The MZM modulates in phase and intensity as response to the voltage signal. The electrical field of the incoming optical carrier can be modulated in phase by applying an external voltage via a coated electrode, utilizing the fact that is possible to change the refractive index of a material and thus the refractive index of the waveguide. It can be considered that the change of the refracted index is linear to the applied external voltage $u(t)$. A driving voltage necessary to obtain a phase shift of π, is denoted by V_π. Thus, the expression that lists the incoming optical carrier and the outgoing phase modulated optical field, is given by [18]:

$$E_{out}(t) = E_{in}(t)e^{j\frac{u(t)}{V_\pi}\pi} \tag{2.9}$$

To cause an intensity modulation of the optical lightwave, the process of phase modulation can also be used by utilizing the principle of interference. This is known by a dual-drive MZM, because both arms can be driven independently (Figure 2.16). The incoming light is split into two paths and acquiring some phase differences relative to each other, then the optical fields are recombined. The relative phase shift can do interference that can vary between constructive and destructive.

The input light is split into two beams through a Y-junction. Each beam goes through the phase modulator of each arm. The drive voltage of each arm is specified by [17]:

$$u_i(t) = V_{bias\ i} + V_{RF\ i}\ ,\ i = 1, 2 \tag{2.10}$$

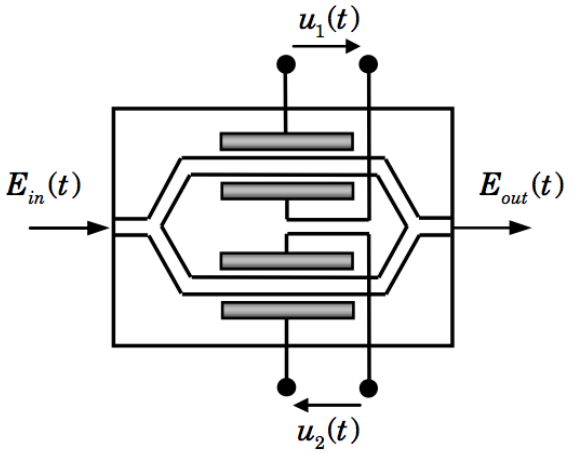


Figure 2.16: Integrated optical Mach-Zehnder modulador (dual-drive) [17].

The MZM can operate in two modes: the push-push mode and the push-pull mode. In the push-push mode it is applied the same phase shift in both arms, it means that $u_1(t) = u_2(t)$. In the push-pull mode the phase is symmetric in both arms and a chirp-free amplitude modulation is obtained, thus $u_1(t) = -u_2(t)$. The expression of the output field can then be written as [17]:

$$E_{out}(t) = \cos\left(\frac{u(t)}{2V_\pi}\pi\right) E_{in}(t) \tag{2.11}$$

From the previous expression, it is possible to conclude that the MZM in push-pull operation is periodic with a period of $2V_\pi$.

The MZM can be biased in two points of the operation curvature: quadrature point and minimum transmission point. In Figure 2.17 is presented these two modes. When the MZM is operating at the quadrature point, the bias voltage, V_{bias} is half of V_π. In this mode the total voltage swing will be equal to V_π. With the MZM biased at the minimum transmission point, the driving voltage will vary a total of $2V_\pi$ with the operating point corresponding to no optical power [17].

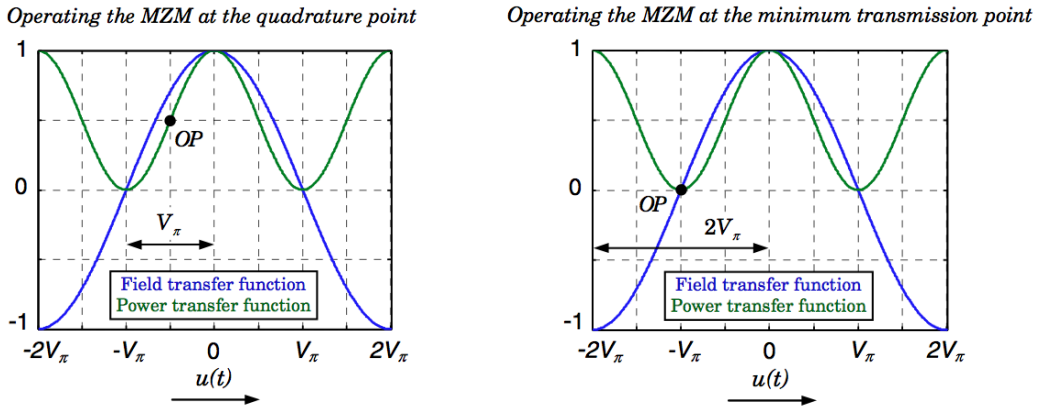
Operating the MZM in push-pull mode leads to the possibility to build an IQ modulator. This type of modulator is shown in Figure 2.18.

With an IQ modulator is possible to modulate signals with high-order modulation formats, due to the disposal of two modulators: the in-phase (I) and the quadrature (Q). To the quadrature part, a phase shift of $\frac{\pi}{2}$ is added, so then there is the necessary difference of phase between the two modulators. The corresponding modulators have the operation point at the minimum transmission point, in order to provide the full constellation.

The amplitude modulation and phase modulation are given by the following expressions [17]:

$$a_{IQM}(t) = \left|\frac{E_{out}(t)}{E_{in}(t)}\right| = \frac{1}{2}\sqrt{\cos^2\left(\frac{u_1(t)}{2V_\pi}\pi\right) + \cos^2\left(\frac{u_Q(t)}{2V_\pi}\pi\right)} \tag{2.12}$$

$$\phi_{IQM}(t) = arg\left[\cos\left(\frac{u_1(t)}{2V_\pi}\pi\right) + \cos\left(\frac{u_Q(t)}{2V_\pi}\pi\right)\right] \tag{2.13}$$



(a) MZM Operation in the quadrature point.

(b) MZM Operation in the minimum transmission point.

Figure 2.17: MZM Operation in the quadrature point and the minimum transmission point [17].

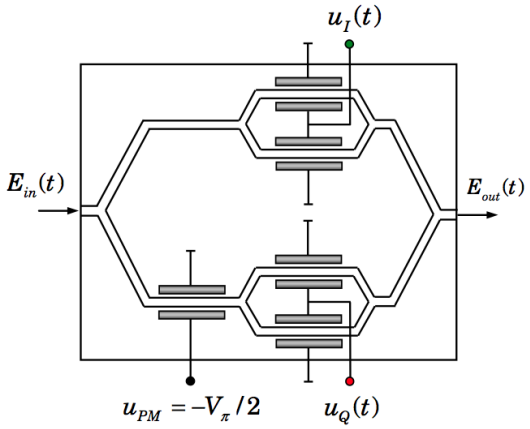


Figure 2.18: Optical IQ Modulator [17].

2.4.5 Photodetectors

Photodetector is an essential component of an optical communication system where an optical signal is converted into an electrical signal to be subsequently amplified by the receiver. The block diagram of an optical receiver system is shown in Figure 2.19 [19].

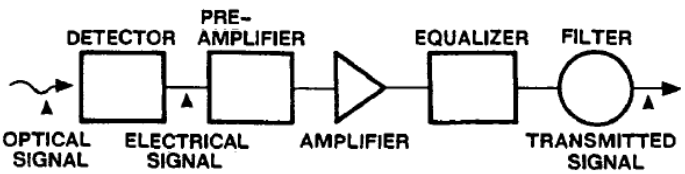


Figure 2.19: Schematic block diagram of a digital optic receiver [19].

It works based on the principle of sensing the response of the material when the electrical carriers are excited by the incident optical radiation. The light absorption process in a semiconductor photodetector for photogeneration of electron–hole pairs is based on the internal photoelectric effect and requires the photon energy $h\nu$ to be at least equal to the bandgap energy Eg of the absorber material. Flow of the photogenerated electrons and holes (created due to the vacancy left in the valence band by the excited electrons) within the material under an externally applied electrical field gives rise to a current (photocurrent) in the external circuit [20].

The responsivity (R) of the detector, defined as the ratio of the photocurrent to the absorbed optical energy, depends critically on the absorption spectrum of the semiconducting material. For high responsivity, the absorbing material should have a bandgap very near, but above the high wavelength limit of the optical signal. Figure 2.20 shows the absorption characteristics of some semiconductor materials in the wavelength range of interest [19].

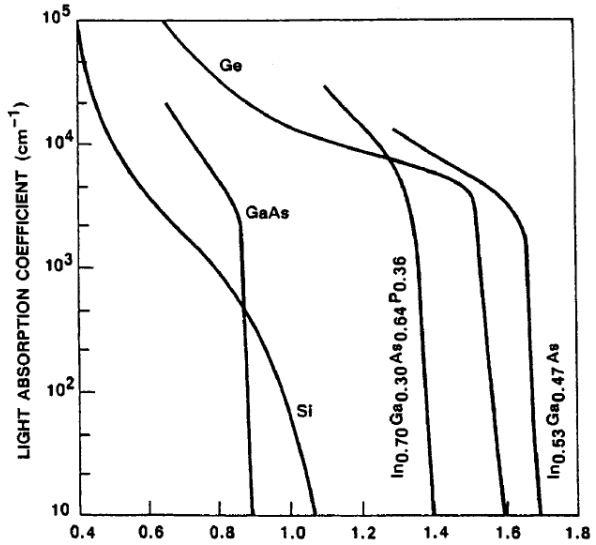


Figure 2.20: Absorption coefficient as a function of wavelength for some important semiconductor materials used in photodetectors [19].

As the photodetector is at the front end of the receiver system, the Signal-to-Noise Ratio (SNR) of the photodetector is the most important in determining the overall noise at the output of the receiver. The high data rate (multi-Gbits/s) of the present-day optical fiber transmission systems puts severe demand on the response speed of the photodetector. Considerable effort has been invested worldwide in developing very high-speed and low-noise optical detectors.

There are essentially three types of photodetectors: PIN (denotes the p-intrinsic-n doping), Metal Semiconductor-metal (MSM) and Avalanche Photodiode (APD). Two of these, the PIN and more recently the MSM photodetectors, have been extensively used for integrated optical receivers. PIN photodetectors are also extensively used in hybrid optical receivers. While there is now an increasing interest on the use of APD it has not yet been used in integrated receivers [21].

2.4.5.1 PIN Photodiode

PIN is the most commonly used photodetector in hybrid optical receivers because of its ease of fabrication, high reliability and biasing compatibility with electronics. The PIN photodetector consists of an intrinsic absorber, inserted between highly doped n^+ and p^+ layers which give rise to a space charge region. Compared to a simple p-n junction, this design allows for a smaller junction capacitance and provides an additional flexibility in designing the thickness of the depleted high-field region [19].

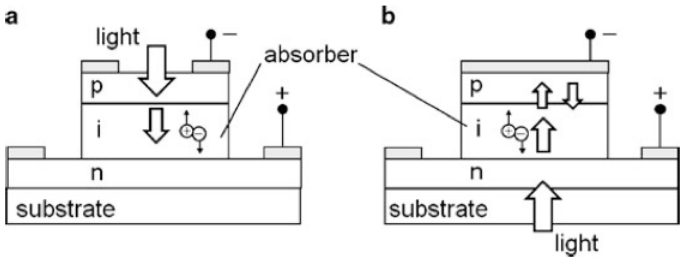


Figure 2.21: Cross-section PIN Photodiode. (a) Top illuminated PIN. (b) Back illuminated PIN [20].

Different types of detection in the PIN photodiode can be seen in Figure 2.21. The top illuminated PIN has become a standard commercial product. For high-speed operation the device is reverse biased by an externally applied voltage to completely deplete the absorber and create an electric field to enable carrier transport. Once an electron–hole pair is created, the carriers drift in opposite directions toward the electrodes and contribute to the photocurrent. It is well known that for this device structure there is a performance trade-off between quantum efficiency and bandwidth associated with the thickness of the absorber region. For a thicker absorption layer, higher quantum efficiency will occur. Although, this will result in longer carrier transit time, reducing the bandwidth. Another factor that reduces the bandwidth is the RC model of the photodetector. Different ways of improving the quantum efficiency keeping high speeds were explored with different layer thicknesses and changing the active junction area to minimize capacitance. Another way is using the back illuminated PIN presented in Figure 2.21 [19].

2.4.5.2 Metal Semiconductor-metal (MSM) Photodetector

Metal Semiconductor-metal (MSM) is a simple device with a planar structure and it consists of a undoped semiconductor absorption layer with a pair of interdigitated metal electrodes that have been deposited on top. Basically, it operates as two Schottky diodes connected back-to-back. One of the contacts is in reverse bias which fully depletes the intrinsic or undoped semiconductor underneath, while the other contact is forward biased. In order to work, a voltage has to be applied to the electrodes to completely deplete the absorber and generate an electric field inside the absorber, as can be seen in Figure 2.22 [19].

The device operates in the same way as a PIN photodetector, with the exception of the implementation and positioning of the contacts. Using lateral contacts, it leads to photodetectors with lower capacitances, by reducing the parallel plate capacitance of the contacts to only edge capacitances. Moreover, this type of photodetectors is well suited for monolithic integration with Metal Semiconductor Field Effect Transistors (MESFET).

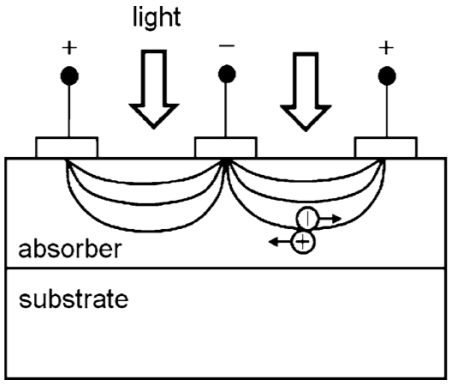


Figure 2.22: Cross-section of the MSM Photodetector [20].

The bandwidth that is limited by the transit time can be enhanced when the finger spacing is narrowed. Still, this enhancement is limited to the point when the finger spacing becomes comparable to the finger width. At this point, the MSM photodetectors suffer from the same fundamental trade-off as the APD and PIN. A type of MSM photodetectors that suffers from even longer transit times is the back illuminated. This happens because the carriers are mainly generated far away from the high electric field regions close to the top electrodes. Thus, when compared with the front-illuminated MSMs, lower bandwidths are shown. This reduction can be as high as 50% [19].

In terms of responsivity, it is considerably lower in the top illuminated, when comparing PIN photodetectors with MSM photodetectors. This fact is due to the interdigitated contact fingers that produce a considerable masking effect. One solution is using semitransparent electrodes, like cadmium tin oxide or thin metal, or by back illumination. The used of black illumination through the substrate can increase the responsivity to the double [19].

MSMs were first used in GaAs for integration with GaAs MESFETs for short wavelength optical receivers. For long wavelength applications, MSM photodetectors with a narrow-bandgap InGaAs absorber are required. However, it is not possible to make good Schottky barrier contacts in InGaAs which has good barrier height and low reverse leakage current suitable for MSM applications. To solve this problem it has been studied some methods to overcome the low Schottky barrier problem on InGaAs and several successful long wavelength integrated receivers have been reported using MSM photodetectors. The most popular approach to produce a usable Schottky barrier on InGaAs is to grow a thin undoped barrier-enhancement layer (GaAs, InAlAs or InP) between the electrode and the absorption layer. Another way is by using p-n juntions instead of Schottky contacts. The n-contact is an alloyed ohmic metallization on InGaAs that is diffused or ion implanted [20].

2.4.5.3 Avalanche Photodiode (APD)

Avalanche Photodiode (APD) is a device with a great sensitivity at lower frequencies due to an internal gain mechanism. Compared to the PIN photodiodes, it has better sensitivity, so it could be used without optical amplifiers. However, the gain process requires some time to settle, deteriorating the temporal response [19].

An APD operates in reverse bias. This reverse bias has to be high enough to cause photon generated carriers, through a high electric field that is established within the depletion region

where electron-hole pairs are generated under photoexcitation. Thus, a single photon is able to generate new electron–hole pairs by impact ionization. This impact ionization process causes the internal gain in the photodetector, but also produces an extra internal noise source compared to the PIN and MSM. Additionally, the excess noise also affects the speed of an APD through the avalanche build-up time, which rises its gain-bandwidth product.

There are different methods created to achieve the low excess noise in an APD. The most popular approach is to select a material with low-noise characteristics such as Si, that has $k << 1$ [19]. However, at long wavelengths tunneling at the high electric fields it is necessary more sophisticated structures that involve the use of separate absorption and multiplication regions, named as SAM-APD. The basic idea behind this is that the electric field must be high enough to cause avalanche multiplication. For this reason, the usage of APDs in integrated receivers is difficult to implement, as they need biasing of tens of volts, hardly compatible with integrated electronics. Moreover, their complexity is also a disadvantage for the integration. Currently, APDs have a gain bandwidth product in the range of 70 GHz to 80 GHz, that corresponds to a operation bandwidth of around 10 GHz [21]. For a single type of ionization carrier, the response time is fastest and the gain-bandwidth product can thus be improved by increasing the ionization coefficient ratio. In the APD is essential the high field to create gain, so it can cause tunneling to occur in the narrow-bandgap InGaAs, that result in high dark current which is undesirable for low bit rate applications.

Although APDs need more complex epitaxial wafer structures and bias circuits, there are already successfully experiments of optical receivers that can operate up to 10 Gbit/s [20].

Chapter 3

Development of the Transceiver Architecture

Introduced the idea in Chapter 2, there is a huge necessity to improve the current optical technologies for future requirements. This dissertation has as main focus the development of a new architecture for the transmitter and receiver devices, so important for the overall system. These advancements on the terminal devices, OLT and ONU, are important for several purposes like greater capability for high data rates, longer range, reliability and costs reduction.

In this chapter some architectures will be studied and presented as candidates for the implementation of the transceiver for NG-PON2 applications. The technology used for the PIC development is SMART Photonics. Then, one architecture will be selected from the ones analyzed to be simulated in detail and implemented in this work. For the selection of the right architecture it has to be considered that the transceiver has the main purpose of being universal as much as possible, that is to be able to be used as OLT and ONU and for both transmission and reception with only one optical interface. Furthermore, the transceiver has to be able to be tuned for different channels for Downstream and Upstream.

Due to this former feature of being able to multiplex and demultiplex the optical signals, the key components of the transceiver are the AWGs. The AWGs are part of the process of light generation inside the chip, because at the same time the light is created, its wavelength has to be selected to the desired channel. The AWG has the role to filter the selected channels inside the cavity, that is a Fabry-Pérot interferometer.

3.1 Aspic™ Simulator

In this work, one of the applications used was Aspic™. Aspic™ is a simulator for the analysis, the modeling and the design of photonics integrated circuits. In Aspic™, circuits are built as a collection of building blocks that do not need the description at physical level. Its model-based approach allows a high abstraction level, focusing on circuit functionality and performance [22].

In Aspic™ software is possible to:

- Calculate the spectral behavior of simple devices and complete circuits;
- Analyze arbitrarily large optical circuits including planar and hybrid building blocks;

- Synthesize complex circuits;
- Export circuits for mask layout generation;
- Compare measurements and simulations for parameter extraction.

SMART photonics technology provides PDK libraries for Aspic™ that makes possible for the designer to built passive components based on process specifications. This allows to, after the component design, do simulations and check the results with the desired requirements.

As mentioned before, for the design of the transceiver, specifically the laser cavity, AWGs are a key part of the functionality. To have accuracy in the results of the simulation for future implementation, the usage of Aspic™ takes an important role, so then the parameters and dimensions of the AWGs are well chosen.

3.2 Fabry-Pérot Interferometer

Fabry-Pérot Interferometer is considered as one of the simplest interferometer devices. It is composed by two parallel highly-reflective low-loss mirrors that may be flat or spherical, with a distance between them of few micrometers and a material with index of refraction n.

A laser based on a Fabry-Pérot Interferometer is a multiple beam interference, that works with a active medium (i.e gain), a energy pump (i.e current source), optical resonator (i.e cavity) and has losses within the material of the waveguides. The ideal single-cavity Fabry-Pérot laser may be thought as an optical resonator as shown in Figure 3.1. The Fabry-Pérot mirrors form an optical cavity in which successive reflections create multiple beam interference fringes.

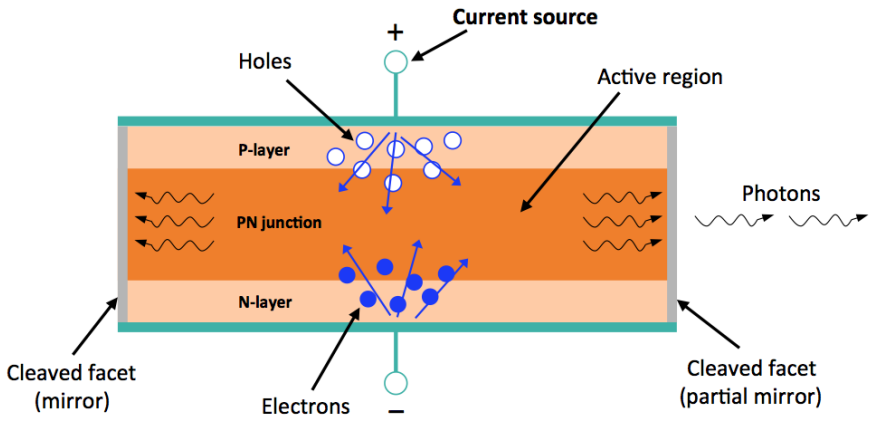


Figure 3.1: Fabry-Pérot Laser (longitudinal section).

The light is created inside the device and the portions of the light will be partially reflected from the surface and kept inside the cavity. Part of the light inside the cavity will become incident on the second reflecting surface, so the portions will be reflected and transmitted. The light transmitted through the second surface and the reflected light, that stays in the cavity, causes a phase difference. The light that is transmitted through the second surface is the output of the laser that can be used for transmission [23].

To control the interference of the light exiting the Fabry-Pérot Interferometer, the optical path inside the cavity can be manipulated. A change in the phase difference between exiting light rays is cause by a change in the optical path length. Generally it is used a material inside the cavity as a spacer layer to modify the interference pattern.

Inside a based Fabry-Pérot laser the light is amplified by stimulated emission. The optical cavity provides feedback for the active region. Thus, the light is continuously reflected and amplified. To guarantee a stable oscillation state inside the cavity (steady-state oscillation), stimulated emission, two conditions have to be assured. First, the electrical field of the optical signal, after completed one lap inside the cavity, has to have the same phase. Additionally, the electrical field of the optical signal, after the completed lap, has to have the same amplitude or more.

All Fabry-Pérot designs share some common features, but there are important differences which determine the right choice of interferometer for a particular application. The best Fabry-Pérot interferometer for a particular application depends on many factors, including size, stability, tunability, free spectral range, resolution and light gathering power.

Designing Fabry-Pérot lasers in Photonic Integrated Circuits (PICs) is usually done using Semiconductor Optical Amplifiers (SOAs) as the active devices for creating stimulated emission. Because SOAs have a broad spectrum response, the dimensions of the cavity and additional filters are implemented to choose the desired wavelength of the light [24].

3.3 Fabry-Pérot Interferometer Design

The laser cavity has to be designed to support light generation for Downstream and Upstream channels. Back to Chapter 2, it was presented the eight channels available for both Downstream and Upstream. It has to be noted that the NG-PON2 standard determines the usage of a minimum of four channels for each transmission direction and to the best knowledge of the author in real applications only four channels are planned to be used.

For this work, the following channels were selected for the design of the laser cavity:

Table 3.1: Selected channels for Downstream and Upstream transmissions

Downstream		Upstream	
Frequency (THz)	Wavelength (nm)	Frequency (THz)	Wavelength (nm)
187.8	1596.34	195.2	1535.82
187.7	1597.19	195.1	1536.61
187.6	1598.04	195.0	1537.40
187.5	1598.89	194.9	1538.19

Principally, the desired laser has to have the functionality to be selected from one to four channels in parallel in Downstream or Upstream. For Downstream this is a required solution because usually the OLT needs to transmit more than one channel at the same time. For the ONU this feature is optional, since the ONU responds normally using only one channel in Upstream. Although, as the cavity will be designed to be universal and to have the resources to transmit more than one channel in parallel, it could also be possible to transmit more than one in Upstream.

Figure 3.2 shows the selected channels for this work over the light wavelength.

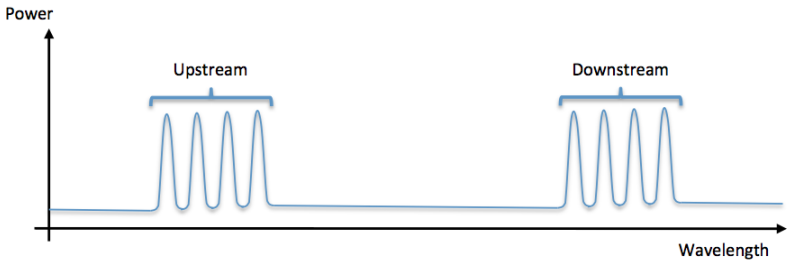


Figure 3.2: Wavelength spectrum of Downstream and Upstream channels.

A block diagram of a conventional laser cavity design incorporating one SOA, one AWG and two Multi-Mode Interference Reflectors (MMIRs) can be seen in Figure 3.3. The AWG is used as a filter to tune the desired output center frequency of the light. The MMIRs are the reflectors in parallel in each end of the cavity. The one located in the end with the output reflects only partially the light, so then the remainder power leads to the output. The other MMIR located on the other side does total reflection for the oscillation. The SOA is the device that gives power gain to create stimulated emission, keeping steady-state oscillation [25].

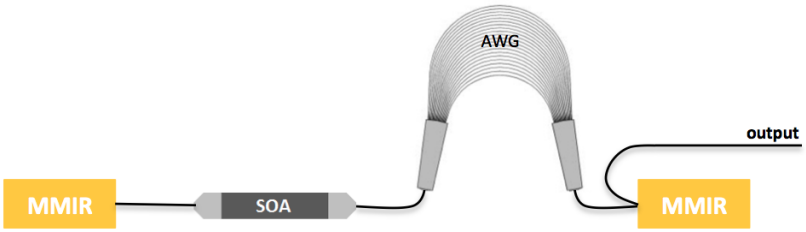


Figure 3.3: Block diagram of a conventional laser cavity.

One can conclude that this conventional architecture will only be valid if only one tone has to be transmitted without any adjustment. So, the proposed way to create several channels from the same cavity has to have several arms with SOAs in parallel joining them in AWGs with more than one inputs / outputs.

3.4 First Architecture Proposal

The first proposal for the laser cavity was based on the idea of having eight arms in parallel, each one corresponding to each channel to be generated (four for Downstream and four for Upstream). Each arm has one SOA and one MMIR in its end, and all arms are joined through one big AWG that multiplexes all channels to one single output.

The block diagram of this architecture is presented in Figure 3.4. With this architecture, the implemented SOAs not only deliver gain to each arm of the cavity but also work as switches to enable or disable the intended channels for the transmission. The MMIRs located on the left end reflect the whole power back to inside the cavity and the MMIR located on the right reflects half the power back to the cavity and the remainder to the output.

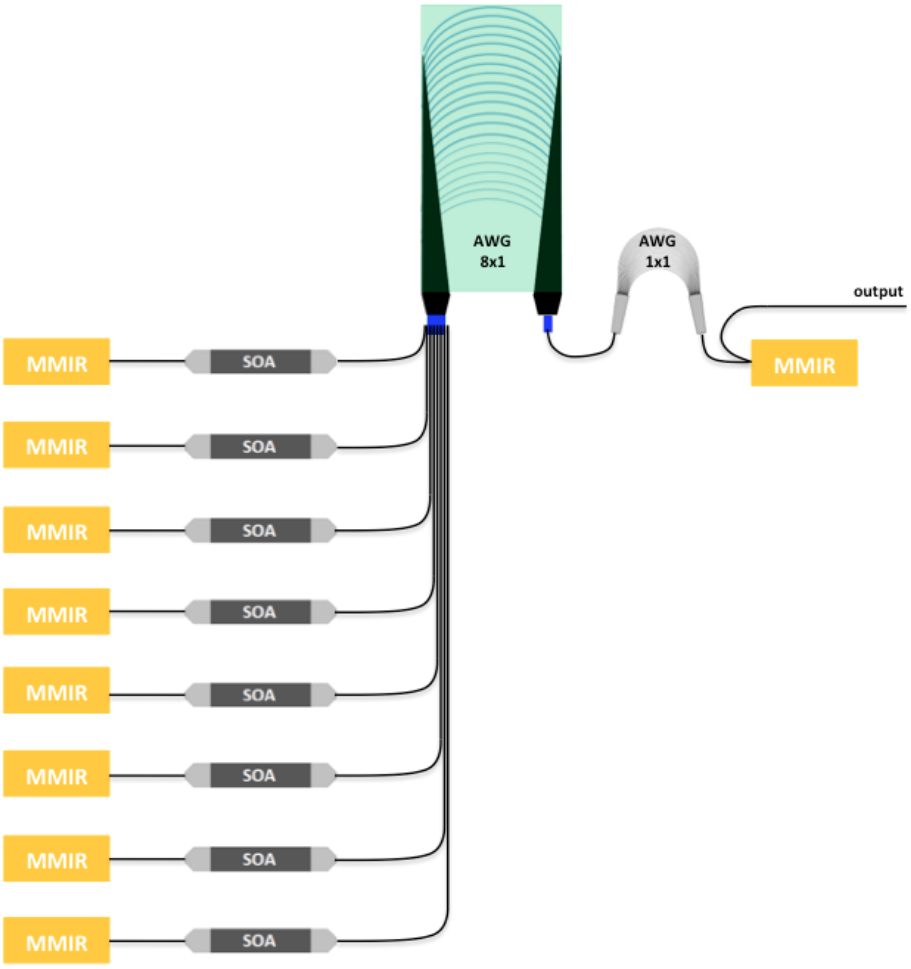


Figure 3.4: Block diagram of the first architecture proposal for the laser cavity.

The two AWGs have different purposes. The bigger one, an AWG with 8 inputs and 1 output (8x1) was designed as a filter for eight channels separated by 100 GHz, that is the separation between channels defined by the standard. Four channels out of these eight (green in Figure 3.5) match the four channels selected for the Downstream and the other four (blue in Figure 3.5), due to the FSR, will match the four channels of the Upstream. This behavior is explained in Figure 3.5.

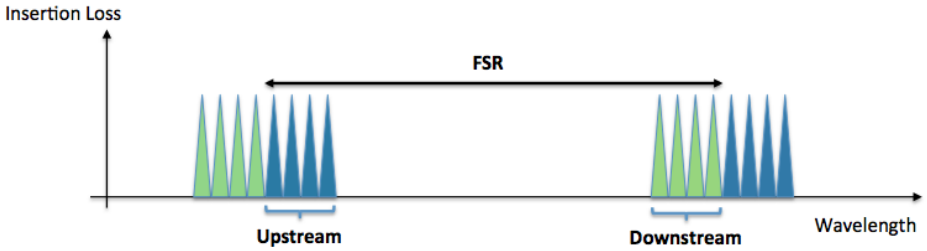


Figure 3.5: Filtering scheme of the AWG 8x1 of the first architecture proposal for the laser cavity.

The other AWG, the smaller one, with only one input and one output (AWG 1x1) was designed as a filter to reject the undesired repeated images. As seen in Figure 3.5, from the resulted 16 images, only 8 are desired for the expected channels. So, this smaller filter has to be able to filter that adjacent images. As expected, this filter would be simple to design, as the response is broad and only has one input. However, accurate precision is necessary in the division between the four desirable images and the four undesirable images. This separation, as mentioned above, is only 100 GHz. The target response for this filter is shown in Figure 3.6.

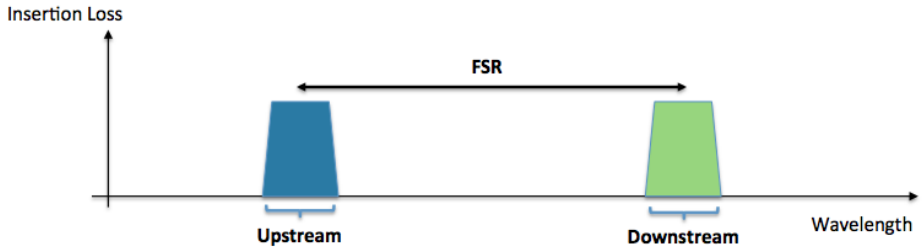


Figure 3.6: Filtering scheme of the AWG 1x1 of the first architecture proposal for the laser cavity.

The light after propagating through the two filters will have the wanted eight channels, four for Downstream and four for Upstream. The total response of the two filters can be seen in Figure 3.7.

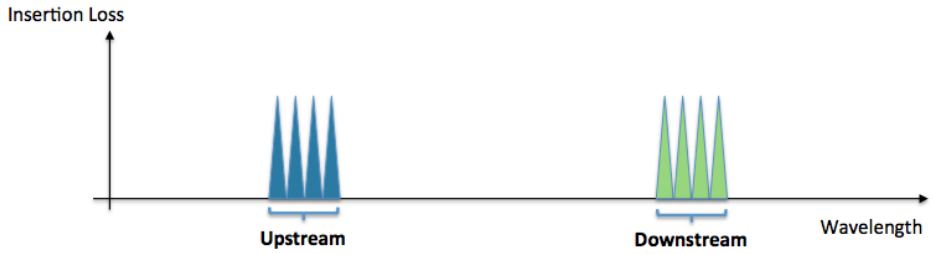


Figure 3.7: Total response of the two AWGs of the first architecture proposal for the laser cavity.

3.4.1 Design and Simulation of AWGs in Aspic™

Using Aspic™ software with the supported PDK from SMART photonics, the wanted AWGs were designed. The AWGs were designed using the AWG cell from COBRA library. Table 3.2 presents the parameters used for the design of the AWG 8x1.

The central wavelength was chosen to be right next to the fourth channel of the Downstream, 1599.74 nm. In this way, four inputs will match the four channels of the Downstream. The FSR is a multiple of the distance necessary to the Upstream. The difference between the central wavelength of the AWG and the center of the repetitions that would match the Upstream is 7800 GHz. With a FSR of 2600 GHz, two additional repetitions will appear in the middle of the filter response. The additional parameters were

chosen for the best filter response that could be achieved, in terms of minimizing the insertion loss and the cross talk.

Table 3.2: AWG 8x1 Design Parameters of the First Proposal

Number of inputs	8
Number of outputs	1
Central Wavelength	1599.74 nm
Channel Spacing	100 GHz
Free Spectral Range (FSR)	2600 GHz
IO waveguide width	2.0 μm
IO waveguide pitch	5.5 μm
Array waveguide width	1.0 μm
Gap between array waveguides at FPR	0.6 μm
Array Acceptance Factor	2.0
Chirp factor	0.0

In Figure 3.8 it can be seen the results of the simulation of this AWG in Aspic™. In Aspic™, simulation after 1600 nm is not supported, so part of the filter response after this wavelength is not seen in the results. From the lobes of the response on the far right, the four of the left are the corresponding to the Downstream. The lobes on the far left, in the range of the 1530s nm, the four of the right are the corresponding to the Upstream. For reference, this Figure can be compared to Figure 3.5. The remaining lobes are repetitions and must be filtered by the following AWG 1x1.

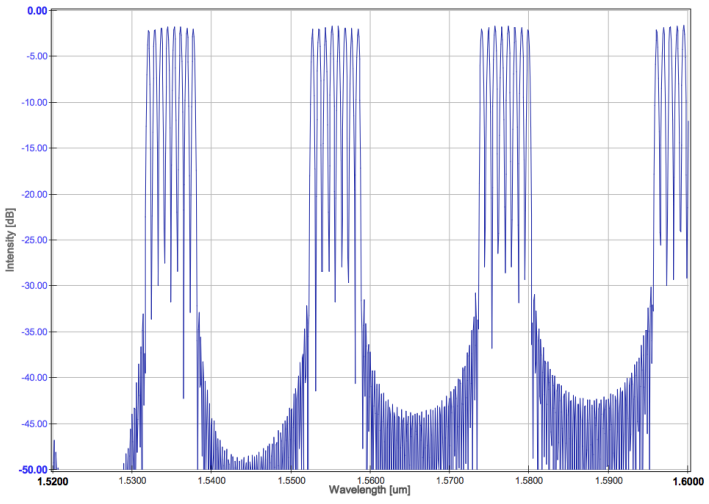


Figure 3.8: Filtering response of the AWG 8x1 of the first architecture proposal. Simulation in Aspic™.

Table 3.3 presents the parameters used for the design of the AWG 1x1. The central wavelength was chosen as a central point of the Downstream channels. The channel spacing parameter influences how wide are the lobes, so it was chosen a relative large value so the four channels would fit inside. The FSR is the distance necessary to the Upstream. This

separation is 7400 GHz and the value of 7350 GHz was obtained as a result of optimization for the best response. The additional parameters were chosen for the best filter response that could be achieved, in terms of minimizing the insertion loss and the cross talk.

Table 3.3: AWG 1x1 Design Parameters of First Proposal

Number of inputs	1
Number of outputs	1
Central Wavelength	1598.04 nm
Channel Spacing	400 GHz
Free Spectral Range (FSR)	7350 GHz
IO waveguide width	3.0 μm
IO waveguide pitch	1.0 μm
Array waveguide width	1.0 μm
Gap between array waveguides at FPR	0.6 μm
Array Acceptance Factor	2.5
Chirp factor	0.0

Figure 3.9 shows the results of the simulation of this AWG in Aspic™. It can be seen that the lobes are centered for Downstream and Upstream. The filter rejection is almost 40 dB and the insertion loss for the pass bands is less than 2 dB.

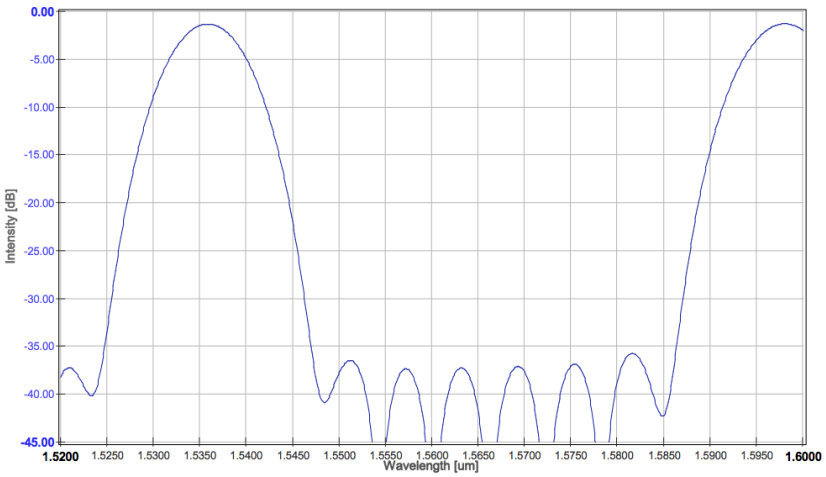


Figure 3.9: Filtering response of the AWG 1x1 of the first architecture proposal. Simulation in Aspic™.

In order to understand if the filters match the requirements, it is necessary to overlap both responses for the complete view. Figure 3.10 presents the response of the two filters together. One can observe that the rejection of the two repetitions in the middle is successfully done. However, the same can not be said about the rejection of the lobes that are next to the channels of interest.

The design of the AWG 1x1 had to accomplish two main requisites, but difficult to fulfill both of them. First, the lobes have to be very wide for the four channels to fit inside, and

sufficiently wide to equalize the insertion loss of all channels. But after the four channels, this AWG has to reject the other four lobes that are corresponding to the repetitions.

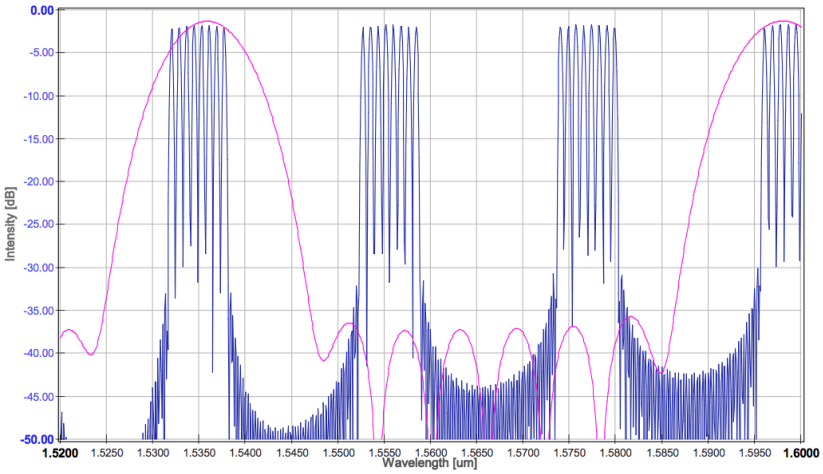


Figure 3.10: Response of the two AWGs of the first architecture proposal. Simulation in Aspic™.

In Figure 3.11 is shown the response of the two AWGs when connected together. Here can be better observed the consequences of the no rejection of the lobes next to the channels of interest.

One example in real application is the following: the SOAs of the Downstream are enabled for Downstream transmission. In this case it will appear only power in four inputs of the AWG 8x1. This power will pass through the pass bands of the desired four channels but also through the lobes on the left next to the Upstream that were not rejected. This is highly undesirable, so one can conclude that this architecture of the laser cavity cannot successfully select the channels for transmission.

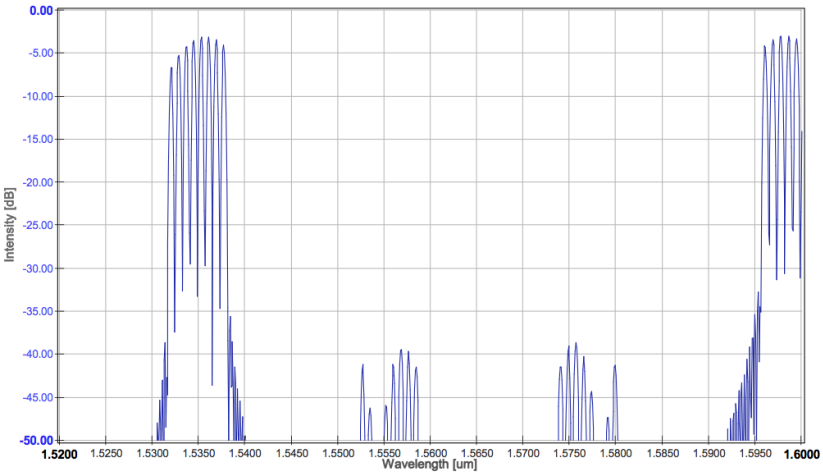


Figure 3.11: Response of the two AWGs when connected together of the first architecture proposal. Simulation in Aspic™.

3.4.2 Remarks about the first architecture

The first proposal for the Fabry-Perót cavity it was successfully designed and demonstrated through simulations. The following remarks conclude the advantages and disadvantages of this approach and the motivation for further proposals:

- The proposed design uses only two AWGs. With the usage of the SOAs as not only amplifiers but also as switches, the cavity has the possibility to select one or more channels for transmission.

- The output wavelengths are determined by the design of the AWGs. In case if other channels for the NG-PON2 standard would be desirable, simple adjustment through redesign of the parameters of the AWGs, like center frequency and FSR, would solve.

- The design has few challenges that would be desirable to overcome with another approach. The need of 8 inputs for the AWG multiplexer forces a large dimension for this component. This could be an important limitation when trying to implement the design on the layout level.

- Another disadvantage is the difficulty of designing the smaller AWG. Although a first look leads to a simple filter, the proximity of the repeated images to the desired channels makes the design very challenging. The response has to be very broad for equal insertion loss of the channels, but it has to filter out sharply and immediately after the passband. The next approach tries to overcome these disadvantages.

3.5 Second Architecture Proposal

From the previous proposal, it was seen that one weakness was the difficulty of designing the smaller AWG to be able to select between Downstream and Upstream due to the proximity between the channels coming from the AWG 8x1. This second proposal has as main goal to find a solution for this problem. Basically, it is necessary to separate Downstream and Upstream way before, so then the channels of Downstream and Upstream are already isolated before the selection being made by the last AWG.

The block diagram of this new architecture is presented in Figure 3.12. In this architecture instead of using a large AWG 8x1 for both Downstream and Upstream channels, it was split in two AWGs, one for each type of transmission. The groups of channels are now well separated in the spectrum, and it is only necessary to take care that the repetitions don't overlap on the bands of interest. So, first the FSR of each AWG 4x1 is chosen to avoid that repetitions are overlapping the spectrum of each other. For example, a replica of Downstream channels cannot fall in the same wavelengths as the group of channels of Upstream.

Coming from the bigger AWGs there are now two waveguides that must be combined for the unique output waveguide, at the same time the replicas have to be filtered out due to the FSR. So, the new small AWG, now with 2 inputs and 1 output, has these two objectives: combine the two outputs coming from the previous AWGs and produce a clean spectrum with only the two required group of channels.

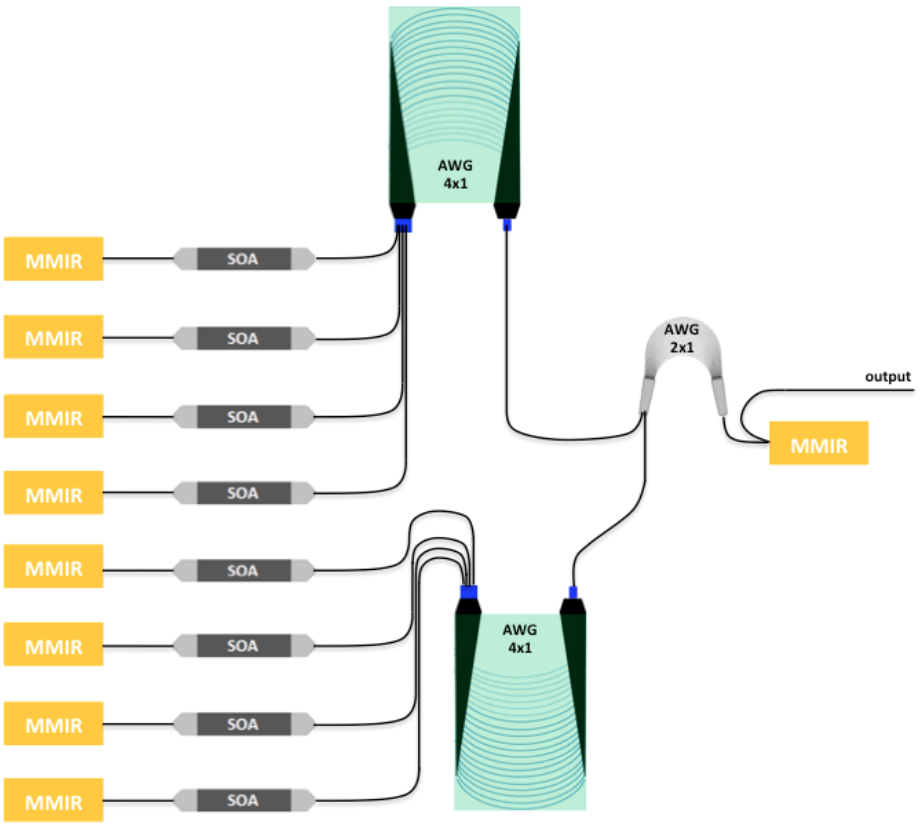


Figure 3.12: Block diagram of the second architecture proposal for the laser cavity.

Figure 3.13 shows the filtering response of the two AWGs 4x1 as one example demonstrating how the replicas cannot overlap the correspondent other band of interest.

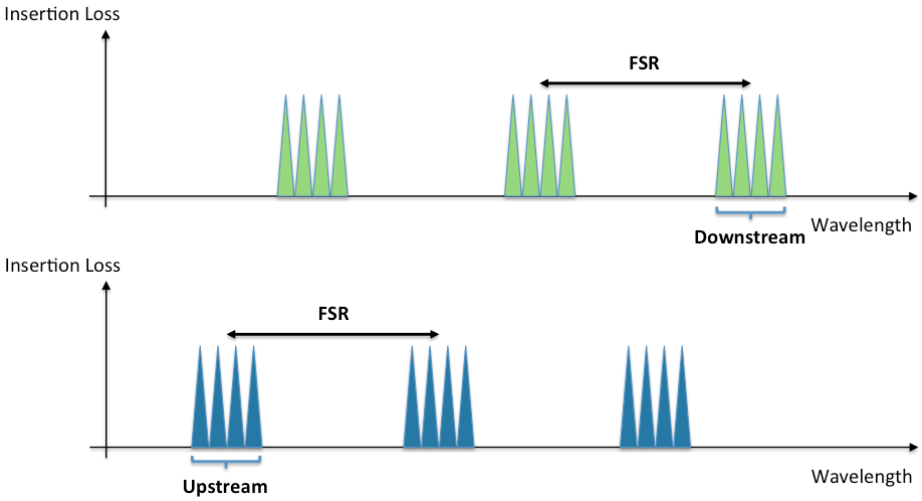


Figure 3.13: Filtering scheme of the AWGs 4x1 of the second architecture proposal for the laser cavity.

Obviously the design of the AWG 2x1 is now much more flexible. Like the AWG 1x1 of the previous architecture, the response of the filter has a broad bandpass to accommodate the four channels of each type of transmission. However, the main difference now is that there is no such fixed 100 GHz of spacing. It should be noted that in the design of the AWGs 4x1, the repetitions of the Downstream and the Upstream were positioned with more spacing to the channels of interest. Thus, on the AWG 2x1 the FSR and the spacing between the two inputs can be chosen with more flexibility. One example of design for this AWG can be seen in Figure 3.14.

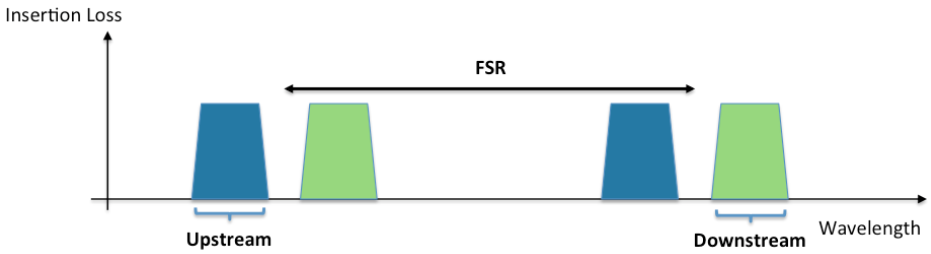


Figure 3.14: Filtering scheme of the AWG 2x1 of the second architecture proposal for the laser cavity.

The light after propagating through the two filters will have the wanted eight channels, four for Downstream and four for Upstream. The total response of the two filters is shown in Figure 3.15.

Figure 3.15: Total response of the three AWGs of the second architecture proposal for the laser cavity.

3.5.1 Design and Simulation of AWGs in Aspic™

Using Aspic™ software with the supported PDK from SMART photonics, the wanted AWGs were designed. As referred before, these AWGs were also designed using the AWG cell from COBRA library.

Table 3.4 presents the parameters used for the design of the AWG 4x1 for Downstream and Table 3.5 for the AWG 4x1 for Upstream.

In case of the AWG for Downstream, the central wavelength was chosen as a central point of the four channels for that transmission. The parameter of channel spacing has a value of 100 GHz, as it is the separation between channels. The value of FSR was chosen to be relatively small, keeping the dimensions of the AWG as low as possible. For the AWG for Upstream all the parameters are similar with exception of the central wavelength that for this

one is the central point of the four channels for that type of transmission. Additionally the value of FSR suffered a little adjustment from 1650 GHz to 1620 GHz. The reason for these values of FSR will be more clear when all the AWGs of this architecture are put together, as they were optimized as consequence of where the lobes of the AWG 2x1 will appear. The additional parameters were chosen for the best filter responses that could be achieved, in terms of minimizing the insertion loss and the cross talk.

Table 3.4: AWG 4x1 for Downstream Design Parameters of Second Proposal

Number of inputs	4
Number of outputs	1
Central Wavelength	1597.6 nm
Channel Spacing	100 GHz
Free Spectral Range (FSR)	1650 GHz
IO waveguide width	3.0 μm
IO waveguide pitch	6.85 μm
Array waveguide width	1.0 μm
Gap between array waveguides at FPR	0.6 μm
Array Acceptance Factor	1.75
Chirp factor	0.0

Table 3.5: AWG 4x1 for Upstream Design Parameters of Second Proposal

Number of inputs	4
Number of outputs	1
Central Wavelength	1537 nm
Channel Spacing	100 GHz
Free Spectral Range (FSR)	1620 GHz
IO waveguide width	3.0 μm
IO waveguide pitch	6.85 μm
Array waveguide width	1.0 μm
Gap between array waveguides at FPR	0.6 μm
Array Acceptance Factor	1.75
Chirp factor	0.0

In Figure 3.16 it can be seen the results of the simulation of the AWG 4x1 for Downstream in Aspic™. Figure 3.17 shows the results of the simulation of the AWG 4x1 for Upstream in Aspic™. As referred before, in Aspic™, simulations after 1600 nm is not supported, so part of the filter response after this wavelength is not seen in the results. In the Downstream filter, the group of lobes in the far right matches the wavelengths of the four channels for that type of transmission. All other lobes are repetitions due to the FSR of the AWG and have to be suppressed by the AWG 2x1. In the response of the Upstream filter, the second group of lobes counting from the left matches the wavelengths of the four channels for that type of transmission. Likewise, all other lobes are repetitions due to the FSR of the AWG and have

to be rejected by the AWG 2x1. These Figures can be compared to Figure 3.13.

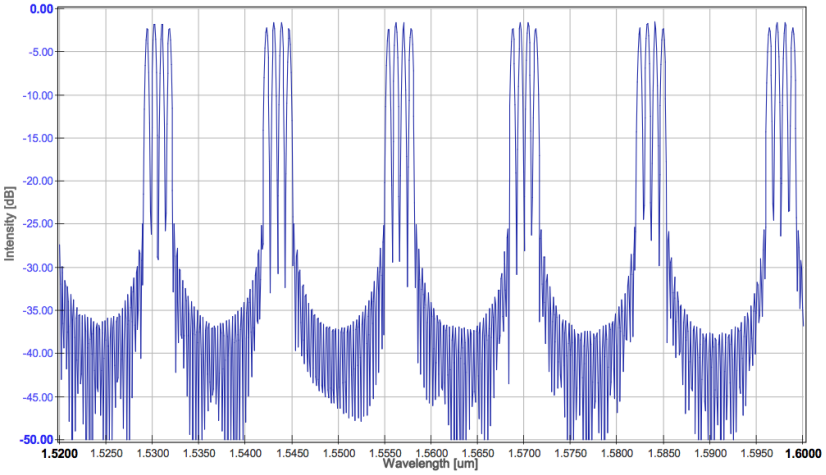


Figure 3.16: Filtering response of the AWG 4x1 for Downstream of the second architecture proposal. Simulation in Aspic™.

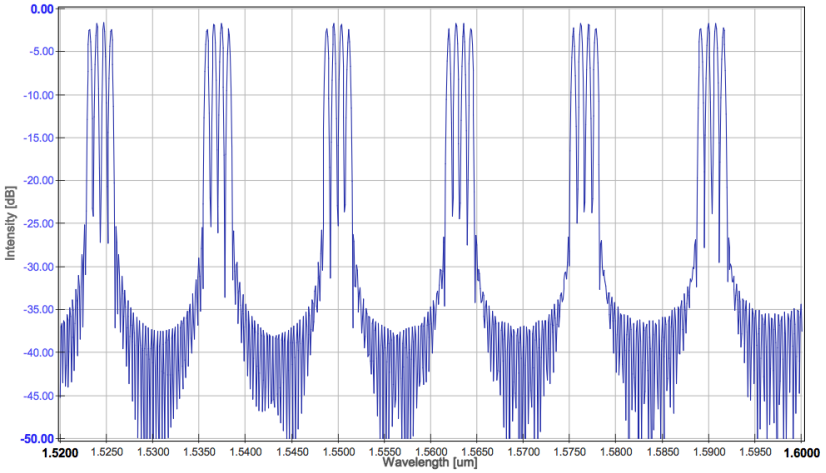


Figure 3.17: Filtering response of the AWG 4x1 for Upstream of the second architecture proposal. Simulation in Aspic™.

Table 3.6 presents the parameters used for the design of the AWG 2x1. This AWG has two inputs, one is chosen for Downstream and the other for Upstream. The corresponding to the Downstream will be the lobe on the right, so the central wavelength has to have a value lower than the wavelengths of the four channels. Additionally, it will depend how wide are the lobes for this value of the central wavelength to be calculated. The width of the lobes is determined by the value of the channel spacing. This value was chosen to be 1700 GHz for the band pass to be relatively wide for equal insertion loss of the channels. The value obtained for the central wavelength was 1590.5 nm. It was used a value of 5600 GHz for the FSR, so that the input corresponding to the left lobe matches the group of four channels of the Upstream. The additional parameters were chosen for the best filter response that could be achieved, in terms of minimizing the insertion loss and the cross talk.

Table 3.6: AWG 2x1 Design Parameters of Second Proposal

Number of inputs	2
Number of outputs	1
Central Wavelength	1590.5 nm
Channel Spacing	1700 GHz
Free Spectral Range (FSR)	5600 GHz
IO waveguide width	3.0 μm
IO waveguide pitch	6.7 μm
Array waveguide width	1.0 μm
Gap between array waveguides at FPR	0.6 μm
Array Acceptance Factor	3.0
Chirp factor	0.0

Figure 3.18 shows the results of the simulation of this AWG in Aspic™. It can be seen that the lobes match the ranges for Downstream and Upstream. The filter rejection is more than 40 dB and the insertion loss for the pass bands is less than 2 dB.

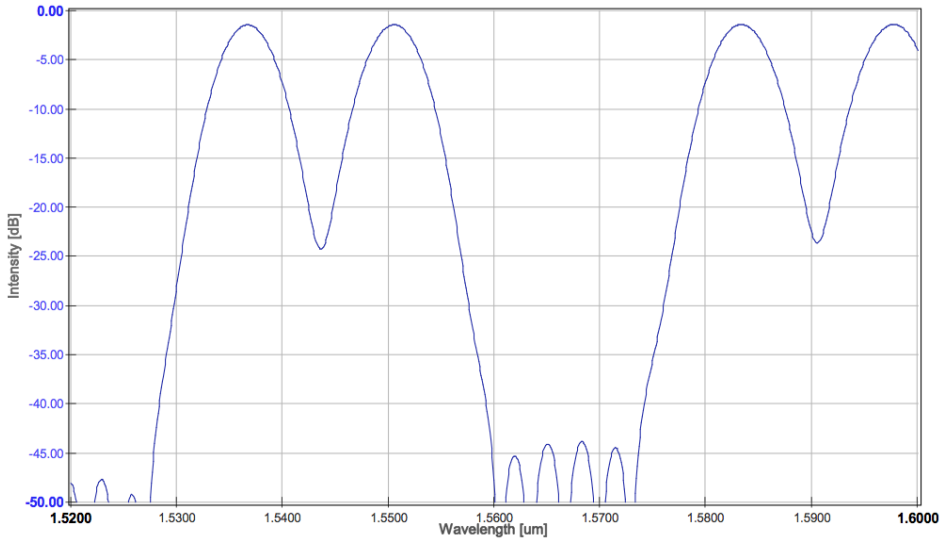


Figure 3.18: Filtering response of the AWG 2x1 of the second architecture proposal. Simulation in Aspic™.

In order to understand if the filters match the requirements, it is necessary to overlap all responses for the complete view. Figure 3.19 presents the response of the three filters together. Several things have to be analyzed through this Figure. First, the right lobe of the AWG 2x1 has to pass successfully the Downstream (in blue) and the corresponding right lobe on the left repetition has to reject the Downstream repetitions. Then, the left lobe of the AWG 2x1 in the far left has to pass successfully the Upstream (in magenta) and the corresponding left lobe on the right repetition has to reject the Upstream repetitions. One important contribution for this to be done successfully was the properly chosen values of the FSR back to the AWGs 4x1.

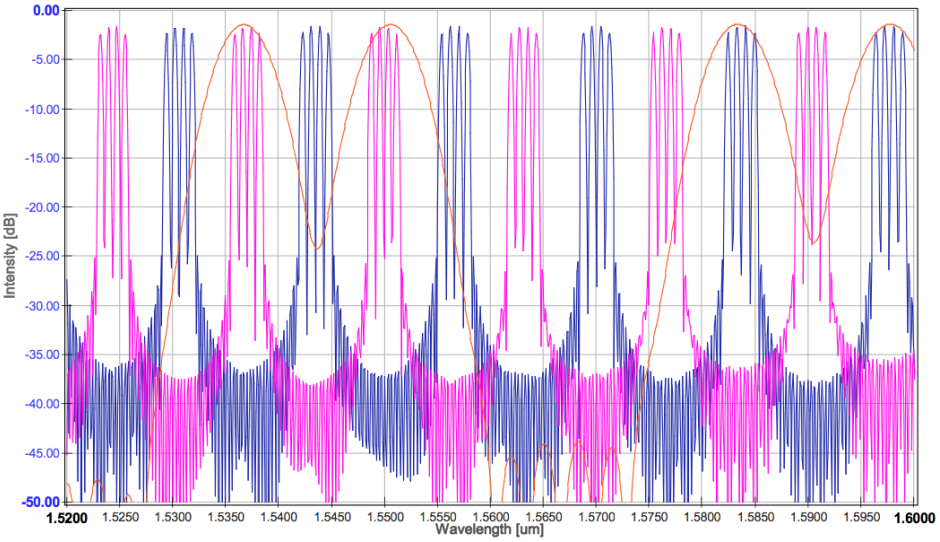


Figure 3.19: Response of the three AWGs of the second architecture proposal. Simulation in Aspic™.

In Figure 3.20 is shown the response of the three AWGs when connected together. Here can be better observed if the three AWGs fulfill all the requirements in terms of passing the channels and rejecting the repetitions.

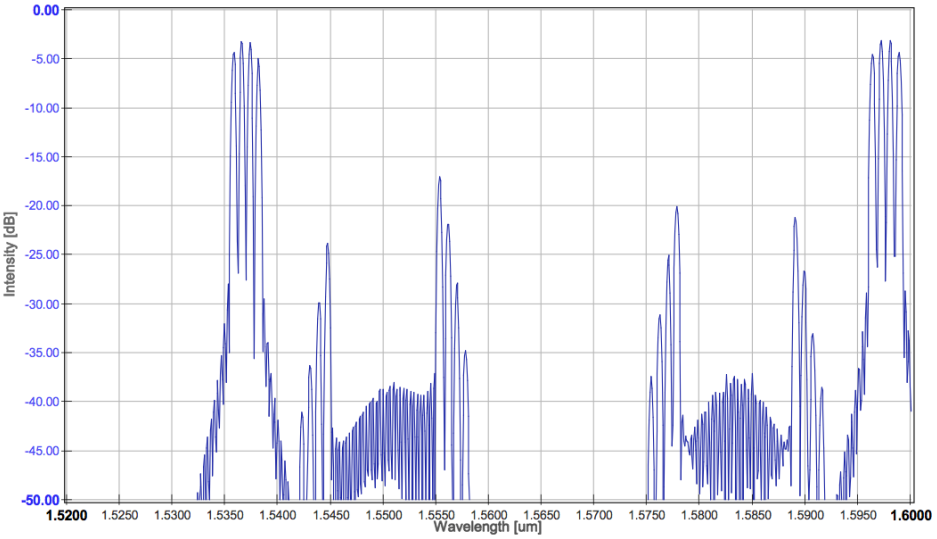


Figure 3.20: Response of the three AWGs when connected together of the second architecture proposal. Simulation in Aspic™.

From this simulation it can be conclude that the rejection is much better when comparing to the first architecture, as the worst value is below -15 dB. The insertion loss of all channels is almost equal, having a difference of around 1 dB. Using this second proposal for the architecture would be possible to have a laser cavity with the possibility of selecting up to eight channels, four for Downstream and four for Upstream.

3.5.2 Remarks about the second architecture

The second proposal for the Fabry-Perót cavity it was successfully designed and demonstrated through simulations. The following remarks conclude the advantages and disadvantages of this approach and the motivation for the final architecture proposal:

- Although the proposed design uses one more AWG, three in total, the two AWGs 4x1 together occupy approximately the same area as the AWG 8x1 of the previous architecture. And, like the previous proposal, with the usage of the SOAs not only as amplifiers but also as switches, the cavity has the possibility to select one or more channels for each type of transmission.

- With this new design it was possible to solve the main issue about the previous one, concerning how tight was to have a successfully filter to select between Downstream and Upstream. Furthermore, with the split of the AWG 8x1 in two AWGs 4x1, the implementation on the layout level can be much more flexible, even if the total occupied area is almost the same.

- Even if it was possible to design these two architectures to create Fabry-Pérot cavities with selectable channels for different types of transmission, other specifications have to be consider in order to proceed with the rest of the design. The main limitation in both designs is that it has only one output of the laser cavity. However this could still work for ONU applications, since that terminal normally only transmits one channel, but in case of the OLT, the transceiver has to be prepared to transmit more than one channel in the wavelength spectrum.

- Having only one output from the laser cavity it limits the possibility of having more than one modulator or photodetector. For having modulation in parallel for different channels, more outputs of the laser cavity are needed. After the modulation, the channels can be combined with a multiplexer for the transmission. Essentially, the architecture of the laser cavity has also to include support for this requirement.

3.6 Final Architecture Proposal

In the design of both previous architectures, the fundamentals of the Fabry-Pérot cavity were explored. Although the architectures were successfully designed and simulated, not all the requirements were achieved when it is applied to the level of the complete transceiver architecture. However, it was an essential procedure to study and learn about how to combine different AWGs to create multiple channels for different types of transmission. It was also analyzed how important is the architecture itself in terms of the combination of different components, when it has to accomplish specifications relative to the low insertion loss and high rejection of the repetitions due to the FSR of the AWGs.

In this section it is proposed the final architecture for the laser cavity that not only matches the specifications in terms of producing different channels of lightwave for the NG-PON2 transmission, that was already achieved in the second proposal, but it introduces the possibility of transmitting in parallel more than one channel. This is essential for the application in the OLT side, that transmits modulated data in several channels that are multiplexed to a single output to reach different users.

The block diagram of the final architecture is presented in Figure 3.21.

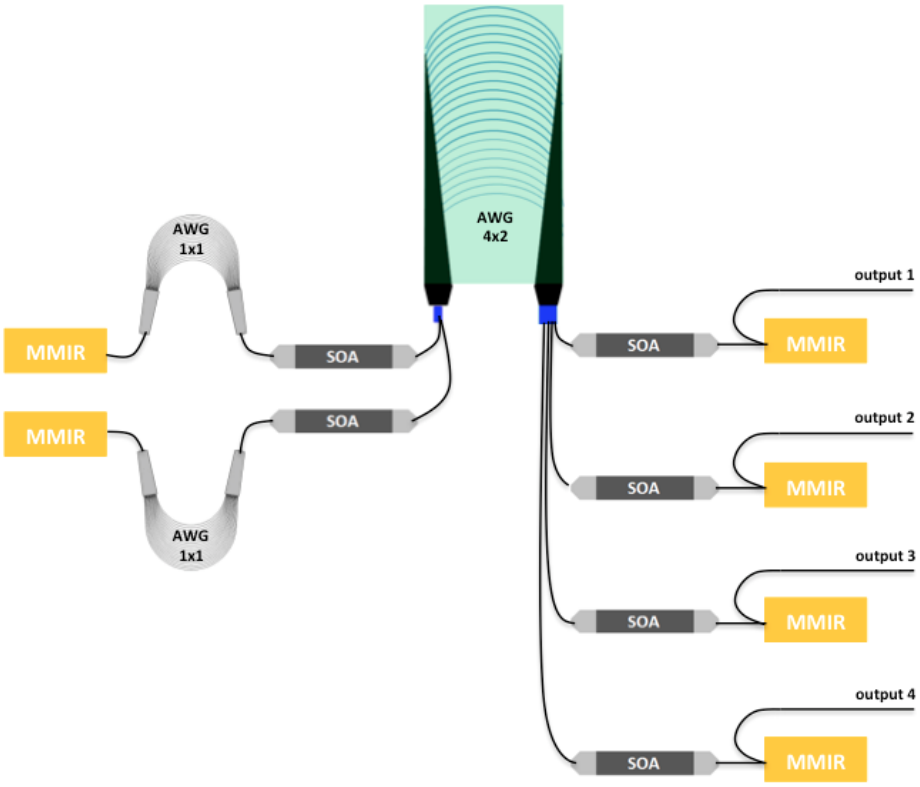


Figure 3.21: Block diagram of the final architecture proposal for the laser cavity.

There are two main differences when comparing to the previous proposals. First, the number of outputs of the laser cavity has now increased to a total of four outputs. As discussed before, this gives the opportunity of having parallel transmissions in different channels. Additionally, the number of SOAs changed from a total of eight to six. This is due to the principle of operation with the new combination of the AWGs that now don't require eight SOAs to create the eight possible channels.

A key component for this topology to work is the introduced AWG 4x2. This is an innovative usage of the AWG properties not only to have several inputs but also more than one output. This unlocks the possibility of splitting the signal coming from the four SOAs in parallel to two branches without using a component like MMI. The response of the AWG not only fits both Downstream and Upstream using the FSR like the previous proposals but delivers the optical signal to two additional SOAs. These two SOAs at the output of the AWG 4x2 select between Downstream and Upstream, since the two type of transmission will never happen simultaneously.

The filtering response of the AWG 4x2 is presented in Figure 3.22. In the Figure is possible to see the two outputs that come from the AWG response. This behavior is explained by the fact that when more than one output is used in the design of AWGs, each output will have the same response but shifted by the same channel spacing used in the design of the inputs. Since the channel spacing used was 100 GHz because of the separation between channels, the outputs have exactly the same response but with the difference of 100 GHz. Now, for the

second output to be able to fit the Upstream channels wavelength, not only the FSR has to be adjusted but it has also to take in account the additional 100 GHz.

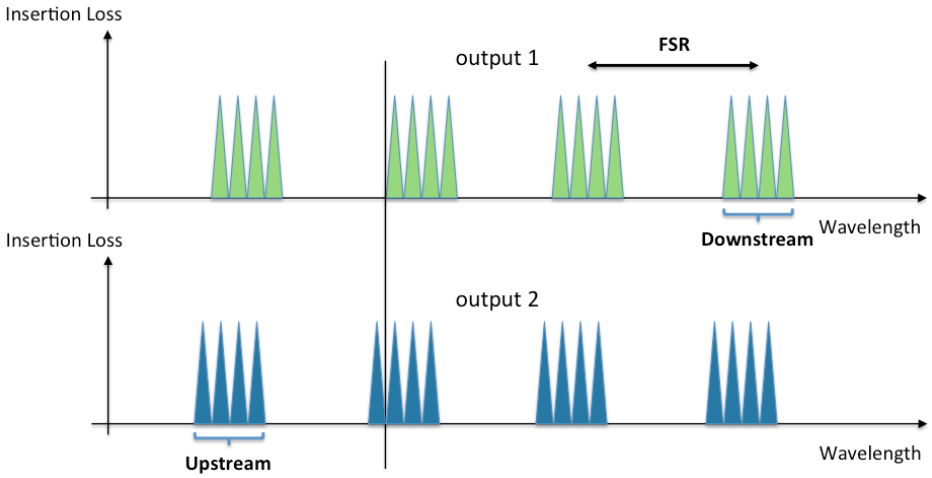


Figure 3.22: Filtering scheme of the AWG 4x2 of the final architecture proposal for the laser cavity.

The design of the small AWGs 1x1 is very straightforward. Both have to have a broad response in order to pass all the four channels together. Then, for each one has to pass either the Downstream channels or the Upstream ones. It has to be taken in account the FSR of them in order to still be able to reject all the repetitions coming from the AWG 4x2. Figure 3.23 shows the filtering response of the two AWGs 1x1.

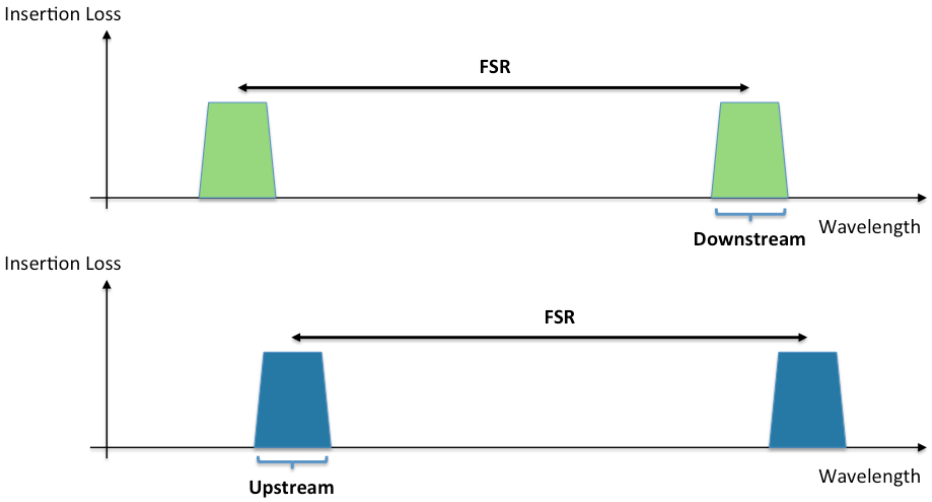


Figure 3.23: Filtering scheme of the AWGs 1x1 of the final architecture proposal for the laser cavity.

They have similar design parameters and responses, but they are designed independently as they are different components. For example, in case of the AWG of the Downstream, the right lobe is the band pass of the four channels of that type of transmission, so they match

the range of wavelengths of the four lobes of the AWG 4x2. The left lobe that is there due to the FSR has to be in one place that will not match any of the repetitions coming from the AWG 4x2 so then these repetitions are rejected inside the cavity. The same principle applies for the AWG 1x1 of the Upstream.

The expected filtering response coming out of the laser cavity through the four outputs available is shown in Figure 3.24.

Figure 3.24: Total response of the three AWGs of the final architecture proposal for the laser cavity.

Finally, the selection of channels in this architecture of the laser cavity will work as following. The SOAs from the right in the laser cavity select the channels to be used in the transmission. It is possible to select from one to four in total. Although it is expected to be only necessary one at time in the operation of the ONU, for the PIC to be universal, i.e compatible with both terminals, when implemented in the OLT it has to have the possibility of selecting more than one channel at time. The two SOAs on the left of the cavity are turned on one at time and will select the type of transmission between Downstream and Upstream. In case the PIC is implemented in an OLT, Downstream must be selected. Otherwise, if the PIC is implemented in an ONU, Upstream must be selected.

In the next chapter, more components will be added to the already presented laser cavity in order to fulfill the whole functionality necessary for the final transceiver. With the whole transceiver structure, the design is presented in more detail and all the necessary simulations will be performed.

Chapter 4

Design and Simulation of the Transceiver

In this chapter, it will be described all the steps of the design and simulation of the transceiver final architecture. Firstly, a block diagram of the complete structure is given. Then, the design and simulation procedure of all the filters that are part of the laser cavity is presented. Furthermore, complete simulations of the transmitter and the receiver are performed using VPItransmissionMaker™. Finally, it is shown the implementation of the PIC layout designed in OptoDesginer.

4.1 Transceiver Block Diagram

In the previous chapter, Chapter 3, it was concluded which architecture to be used in terms of light generation. However that block is only one part of the complete structure needed for the design of the whole transceiver. In Figure 4.1 it is shown the complete block diagram of the transceiver to be designed.

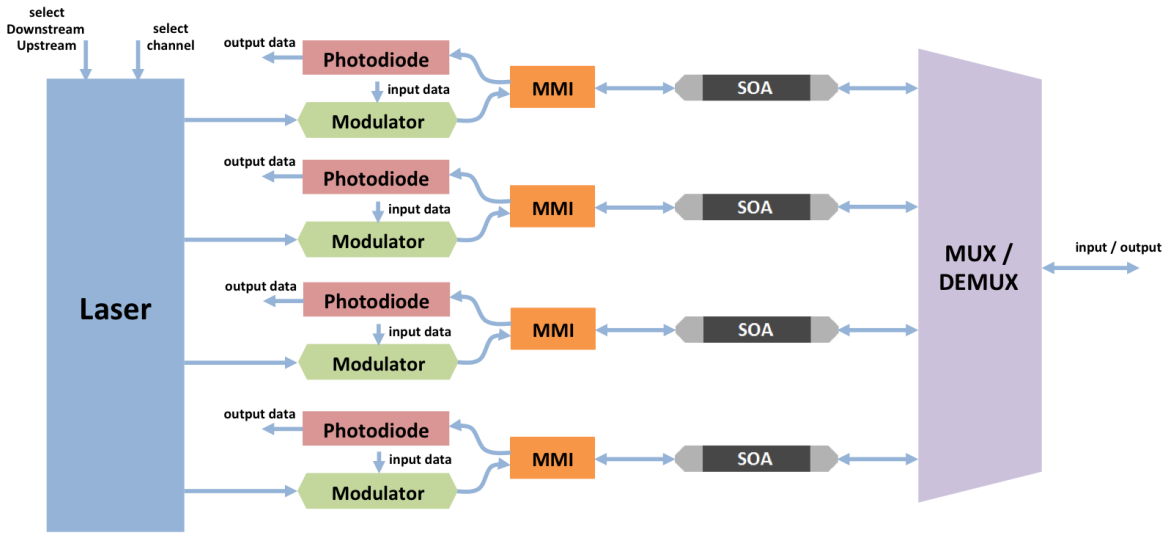


Figure 4.1: Block Diagram of the Transceiver.

From the laser there are four outputs, one for each channel. For each channel, there is a modulator, so then in case of the Downstream, more than one channel can be transmitted simultaneously. After the modulators, the lightwave with the modulated signal is amplified before being transmitted. Finally, all channels are combined through the multiplexer.

When the transceiver is in receiver mode, the light comes from the same interface, identified as input / output, then the signal is demultiplexed and amplified. After the MMI device, the photodiode receives and demodulates the optical signal into an electrical data signal.

4.2 Design and Simulation of the Laser Cavity

The laser cavity has to be designed to support light generation for Downstream and Upstream channels. Back to Chapter 3, it was presented the chosen four channels for Downstream and Upstream transmissions to be supported by the transceiver. In the end of the chapter it was proposed the final architecture of the laser cavity that supports the two directions of transmission and it is compatible with the possibility to transmit more than one channel in parallel, that is an important requirement for the OLT implementation. This architecture was shown in Figure 3.21.

4.2.1 Design and Simulation of AWGs in Aspic™

Using Aspic™ software with the supported PDK from SMART photonics, the wanted AWGs were designed. As referred before, these AWGs were also designed using the AWG cell from COBRA library.

Table 4.1 presents the parameters used for the design of the AWG 4x2. As explained before, this AWG is the key component of this architecture. It has an innovative design, because not only has several inputs but also more than one output. Having two outputs, it will split the signal directly to two different paths, that contain switches to select between Downstream and Upstream transmissions. The central wavelength has the value of the second channel of the Downstream. The reason is because the second output is the one to be used for the Downstream and this output will have a shift of 100 GHz. Due to the FSR, the first output will match the four channels of the Upstream. The value of the FSR is three times less the required difference between Downstream and Upstream. The difference is calculated for example between the third channel of the Downstream and the fourth channel of the Upstream, again because of the shift of 100 GHz between the outputs. This difference is 7300 GHz. Two additional repetitions will appear between Downstream and Upstream due to the value of the FSR (2432 GHz). The additional parameters were chosen for the best filter response that could be achieved, in terms of minimizing the insertion loss and the cross talk.

In Figure 4.2 it can be seen the results of the simulation of the AWG 4x2 in Aspic™. As referred in the previous chapter, in Aspic™ simulation after 1600 nm is not supported, so part of the filter response after this wavelength is not seen in the results. It can be observed the lobes of both outputs: blue corresponds to the first output, used for the Upstream and magenta corresponds to the second output, used for the Downstream. As predicted, there are two repetitions between Upstream and Downstream that need to be filtered by the following AWGs. These results can be compared to the expected response shown in Figure 3.22.

Table 4.1: AWG 4x2 Design Parameters

Number of inputs	4
Number of outputs	2
Central Wavelength	1597.19 nm
Channel Spacing	100 GHz
Free Spectral Range (FSR)	2432 GHz
IO waveguide width	2.0 μm
IO waveguide pitch	5.5 μm
Array waveguide width	1.0 μm
Gap between array waveguides at FPR	0.6 μm
Array Acceptance Factor	2.0
Chirp factor	0.0

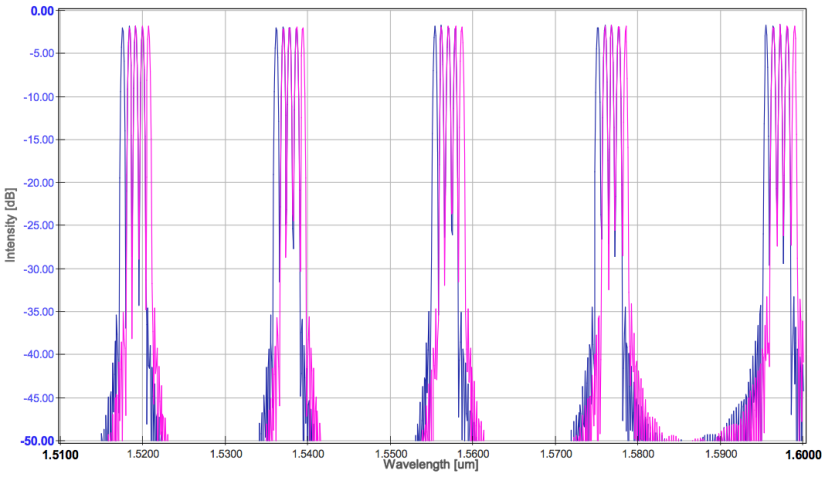


Figure 4.2: Filtering response of the AWG 4x2 used in the laser cavity. Simulation in Aspic™.

Table 4.2 and Table 4.3 show the parameters used for the design of the AWGs 1x1. The first is corresponding to the Downstream and the second to the Upstream. Each one has only one input and one output. The only goal of these AWGs is to reject all the lobes coming from the AWG 4x2 apart of the ones that are in place of the four channels of the corresponding transmission. The AWG 1x1 of the Downstream has as central wavelength the value that is the middle point of the four channels, 1597.615 nm. The channel spacing of 450 GHz was chosen for the passband to be broad in order to pass all the four channels. The FSR had to be high enough for the repetition to be located in a place where no repetitions of the AWG 4x2 were. The AWG 1x1 of the Upstream has similar parameters, with exception of the central wavelength that in this case is the central point of the four channels of this type of transmission. The FSR had a small adjustment too.

Table 4.2: AWG 1x1 for Downstream Design Parameters

Number of inputs	1
Number of outputs	1
Central Wavelength	1597.615 nm
Channel Spacing	450 GHz
Free Spectral Range (FSR)	8250 GHz
IO waveguide width	2.0 μm
IO waveguide pitch	1.0 μm
Array waveguide width	1.0 μm
Gap between array waveguides at FPR	0.6 μm
Array Acceptance Factor	2.5
Chirp factor	0.0

Table 4.3: AWG 1x1 for Upstream Design Parameters

Number of inputs	1
Number of outputs	1
Central Wavelength	1537 nm
Channel Spacing	450 GHz
Free Spectral Range (FSR)	8300 GHz
IO waveguide width	2.0 μm
IO waveguide pitch	1.0 μm
Array waveguide width	1.0 μm
Gap between array waveguides at FPR	0.6 μm
Array Acceptance Factor	2.5
Chirp factor	0.0

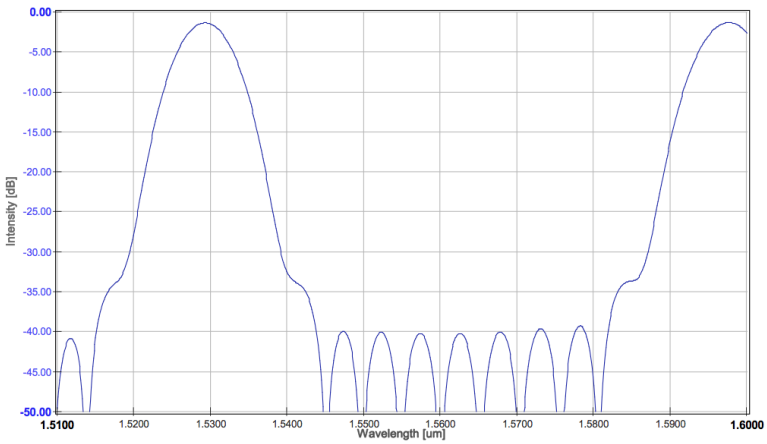


Figure 4.3: Filtering response of the AWG 1x1 for the Downstream used in the laser cavity. Simulation in Aspic™.

Figure 4.3 and Figure 4.4 show the results of the simulation of these AWGs in Aspic™. It can be seen that the lobes match the range for Downstream and Upstream. The filter rejection is more than 35 dB and the insertion loss for the pass bands is less than 2 dB.

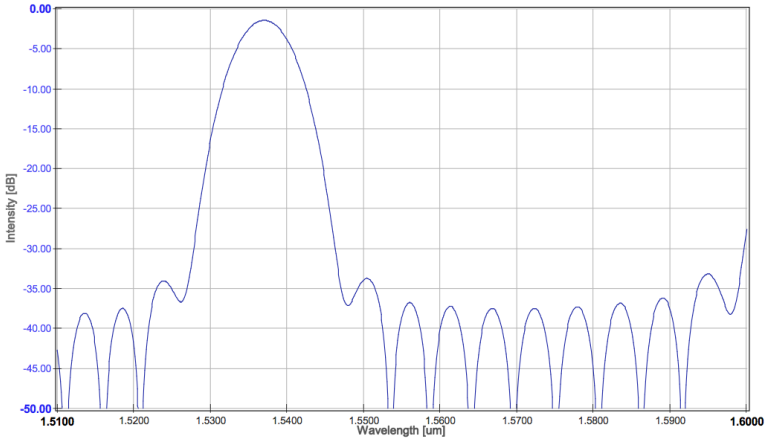


Figure 4.4: Filtering response of the AWG 1x1 for the Upstream used in the laser cavity. Simulation in Aspic™.

In order to understand if the filters match the requirements, it is necessary to overlap all responses for the complete view. Figure 4.5 presents the response of the three filters together. The green shape corresponds to the response of the AWG 1x1 for the Downstream. So, it has to pass only the four lobes in magenta that are in place of the wavelengths of the Downstream. In case of the AWG 1x1 for the Upstream, in orange in the Figure, it has to pass only the four lobes in blue corresponding to the four channels of the Upstream. Everything else, the AWGs have to reject.

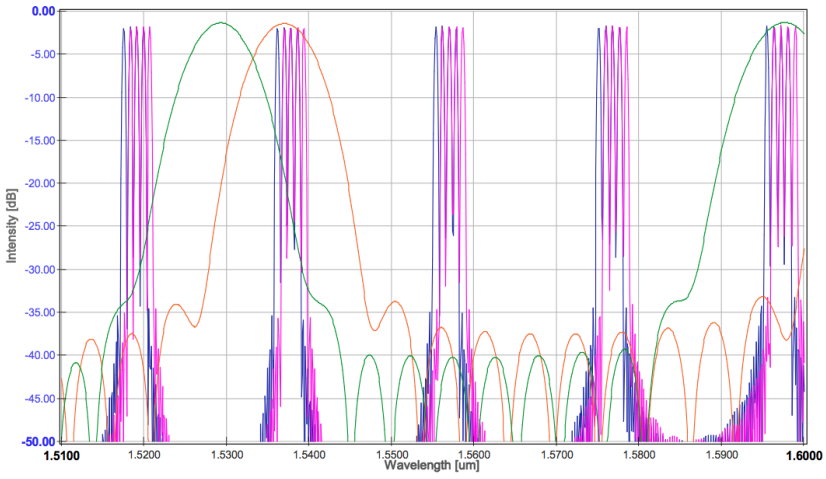


Figure 4.5: Filtering response of the three AWGs used in the laser cavity. Simulation in Aspic™.

In Figure 4.6 it is shown the response of the three AWGs when connected together. Here it can be better observed that the three AWGs fulfill all the requirements in terms of passing the channels and reject the repetitions. One can see that all the repetitions are rejected with a value below -20 dB. The insertion loss difference between the channels is less than 1 dB. These simulations in Aspic™ demonstrate that all the parameters for the design of the AWGs were well chosen and the design of the transceiver can be based in this architecture.

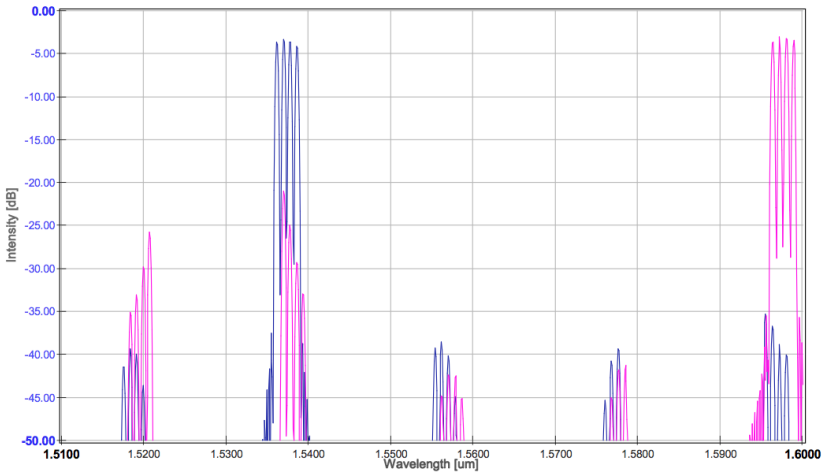


Figure 4.6: Filtering response of the three AWGs used in the laser cavity when connected together. Simulation in Aspic™.

4.2.2 Modeling the SOA in VPItransmissionMaker™

As introduced in Chapter 3, in order to complete the design of the laser cavity, a device that gives power gain to the light is required. This device is the Semiconductor Optical Amplifier (SOA), that is an active optical component. SOA is the building block that creates stimulated emission of light in order to keep a steady-state oscillation inside the cavity. These amplifiers need a certain bias current for their operation. When the bias current is provided, the light is amplified with stimulated emission, and when the current is not given, no light is generated. Through this bias current, it is possible to use these devices as switches. The SOAs, together with the filters and the reflectors, will create the wanted wavelengths at the output of the laser cavity, using the architecture already presented.

In order to build a full simulation setup of the laser cavity, i.e AWGs, MMIRs and SOAs together in the same test bench to emulate the light emission, a model of the SOA was implemented in VPItransmissionMaker™ software. VPItransmissionMaker™ had to be used because in Aspic™ it was not possible to simulate active building blocks. However, there is no PDK available for VPItransmissionMaker™, so a model had to be realized based on the available specifications provided in the SMART photonics process design manual. In Figure 4.7 it is shown the schematic of the test bench used for the SOA testing in simulation.

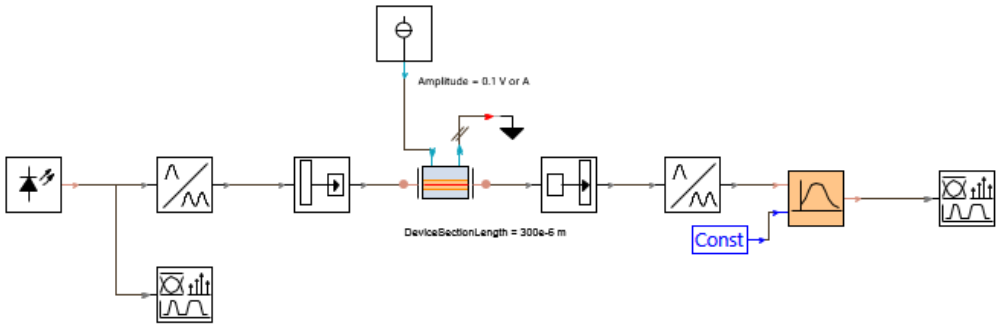


Figure 4.7: Schematic of the SOA test bench in VPItransmissionMaker™.

The modeling of the SOA involves the usage of the SOA component in VPItransmissionMaker™ added to a MATLAB code that runs in parallel. This hybrid solution of using the VPItransmissionMaker™ simulation together with MATLAB is named co-simulation. This co-simulation aims to approximate several specifications given by the design manual [10]. These specifications are represented in Figure 4.8 on the left, as it was already introduced in Chapter 2. This Figure shows the dependency of the gain with the current density over the light wavelength of a SOA with a length of 1200 μm. It would not be enough to develop the SOA model in the simulation using only the SOA block from VPItransmissionMaker™, due to the inaccuracy to match such gain shape. For better precision to fit the gain curve, MATLAB is used to implement equations that can describe that shape. It could be suggested that a block using just MATLAB would be enough, although this would omit other SOA effects such as nonlinear behaviors, gain saturation and spontaneous emission noise. The implementation of this model using co-simulation was developed and explored in [26].

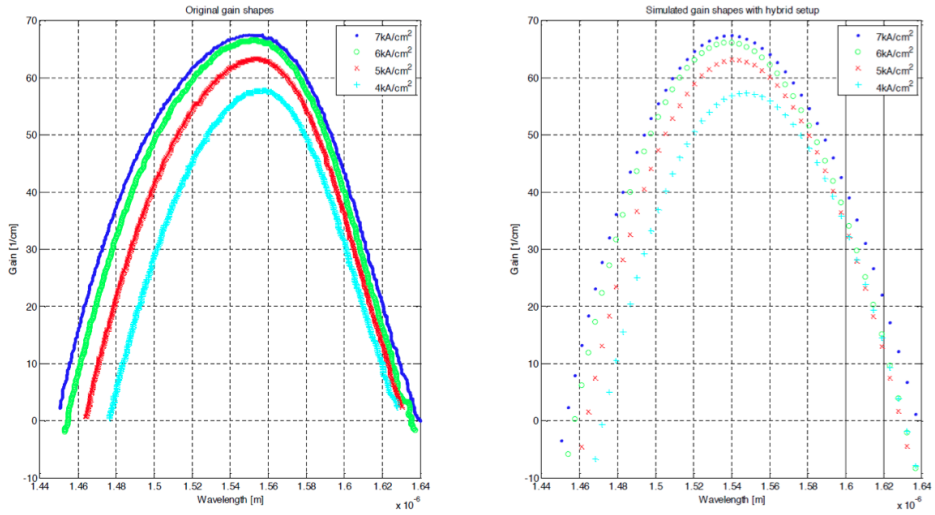


Figure 4.8: SOA gain over wavelength for different current densities. The left figure is the reference from the design manual and the right figure is the simulated gain in the hybrid setup [26].

Figure 4.8 displays the comparison between the shape given by the design manual and the successful realized model of the SOA.

For the transceiver design in this dissertation, the developed model was used with some adapted parameters. One main change in the parameters was the length that was reduced to just 300 μm. The reason for this reduction is because inside the laser cavity two SOAs will be always in series when activated, leading to the conclusion that such length for each SOA would deliver sufficient gain.

Table 4.4 summarizes the main parameters used in the SOA building block in VPItransmissionMaker™.

Table 4.4: SOA Parameters used for the simulation in VPItransmissionMaker™

Current Source	100 mA
Device Section Length	300 μm
Active Region Type	MQW
Active Region Width	2.5 μm
Active Region Thickness MQW	84 nm
Active Region Thickness SCH	208 nm
Confinement Factor MQW	0.054
Confinement Factor SCH	0.56
Optical Coupling Efficiency	0.9772
Gain Shape Model	Parabolic
Gain Coefficient Linear	2.4×10^{-20} m^2
Gain Peak Frequency	194 THz
Gain Bandwidth	22.783 THz
Carrier Density Reference Gain Shape	6×10^{24} m^{-3}
Nonlinear Gain Coefficient	5.5×10^{-23} m^3
Linear Recombination	600×10^{-12} m^{-1}
Bimolecular Recombination	2.62×10^{-16} m^3/s
Auger Recombination	5.27×10^{-41} m^6/s
Initial Carrier Density	5×10^{24} m^{-3}
Spontaneous Emission Noise Bandwidth	10 THz

In the schematic shown in Figure 4.7, it was inserted at the input a total of 16 ideal Continuous Wave (CW) lasers in parallel, instead of only one, to create a spectrum of 16 light wavelengths covering a range from 187 THz to 196 THz with a separation of 600 GHz. The aim of this simulation was to test the performance of the implemented SOA in the frequencies that include the bands of Downstream and Upstream. The power of each wavelength at the input of the SOA is -23 dBm. Figure 4.9 presents the output response of the SOA in that simulation. It is possible to observe the dependency of the gain with the frequency, as for different frequencies the output power is slightly different. This model will be used for the upcoming simulations.

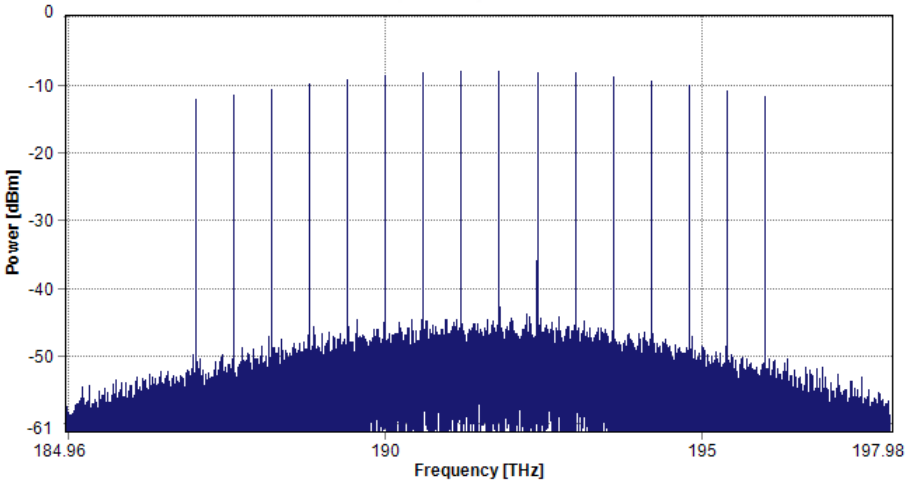


Figure 4.9: Simulation of the SOA model implemented in VPItransmissionMaker™. SOA output power over frequency. The input power used was -23 dBm. It is possible to observe the gain dependency from the frequency.

4.2.3 Simulation of the Laser Cavity in VPItransmissionMaker™

After it was designed the AWGs and modeled the SOA that are part of the process that creates the light emission, it can now be done a complete simulation of the laser cavity.

Figure 4.10 recovers the block diagram of the laser cavity that was explained in detail in Chapter 3. VPItransmissionMaker™ had to be used to perform a complete simulation. This was necessary because in Aspic™ it was not possible to include active building blocks in the simulation. So, with the model of the SOA already implemented in VPItransmissionMaker™, one task that had to be done was the realization of the AWGs in VPItransmissionMaker™ that were designed in Aspic™ before. Finally, the MMIR devices were directly implemented using a building block from VPItransmissionMaker™, named “Reflector”.

The results of the simulation can be seen in Figure 4.11. In this simulation all the channels were enabled, putting all SOAs with the necessary bias current. Although this is not a real case, this simulation aims to show all the channels at the same time to compare the difference of powers among them and to confirm that all the filters are working properly. It can be concluded that the AWGs are performing as expected, as the channels are well defined and the repetitions have a rejection in the range of 50 dB. Some differences in the powers among the channels are observed, in the range of 3 dB to 4 dB. Part of this difference was already observed in Aspic™ simulations due to some difference of insertion loss between channels. In the cavity this difference is enhanced a bit, although it is believed to not be a issue for the system application.

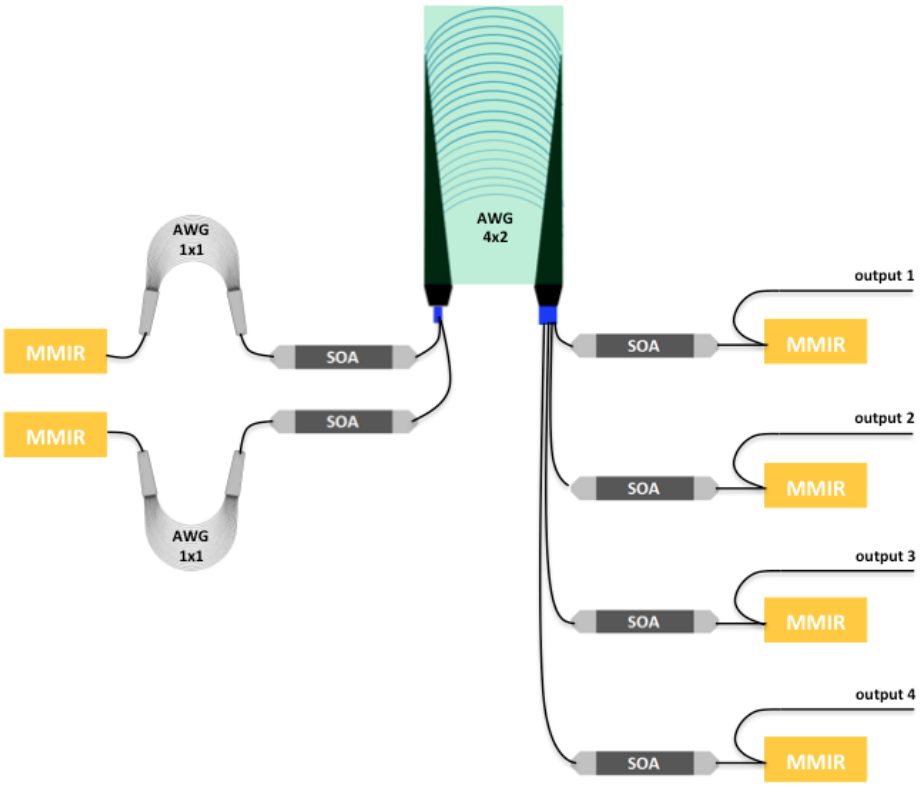


Figure 4.10: Block diagram of the laser cavity.

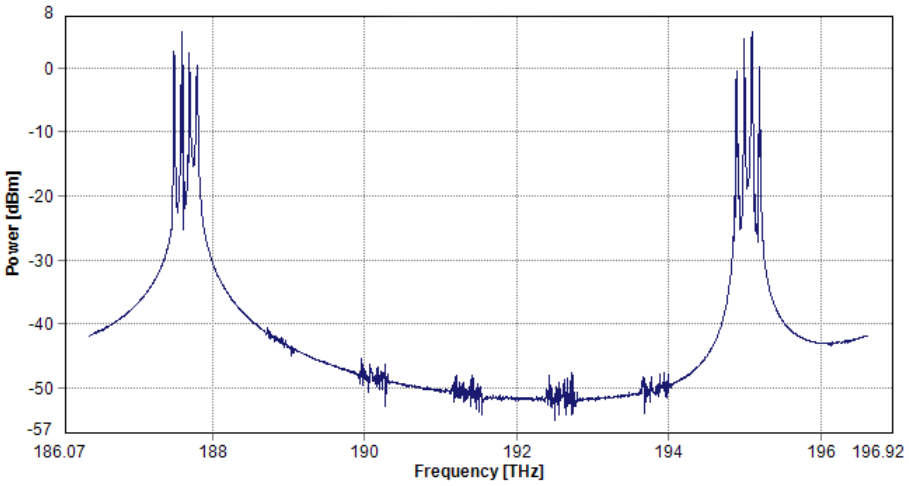


Figure 4.11: Simulation of the laser cavity emitting all channels in VPItransmissionMaker™.

4.3 Design and Simulation of the Multiplexer / Demultiplexer

Now that the design of the laser cavity was successfully completed, more blocks of the transceiver have to be designed and simulated. In this section, it will be presented the several steps of the development of the Multiplexer / Demultiplexer. The role of this block can be seen through the Figure 4.1 shown before. This block will combine a maximum of four signals with modulated data to a unique output of the PIC. When the transceiver is in receiver mode, this block will demultiplex a maximum of four channels received into four different paths that will terminate in the corresponding photodetector.

Using Aspic™ software with the supported PDK from SMART photonics, the wanted AWG was designed. As referred before, this AWG was also designed using the AWG cell from COBRA library.

Table 4.5 presents the parameters used for the design of the multiplexer / demultiplexer, that is an AWG 4x1. The central wavelength has the value that is the central point of the four channels of the Downstream. The value of the FSR is six times less than the required difference between Downstream and Upstream. This difference is 7400 GHz and it is calculated between the center of the Downstream and the center of the Upstream. Due to the FSR, five repetitions will appear between the ranges of the two types of transmission. The additional parameters were chosen for the best filter response that could be achieved, in terms of minimizing the insertion loss and the cross talk.

Table 4.5: AWG 4x1 Design Parameters (Multiplexer / Demultiplexer)

Number of inputs	4
Number of outputs	1
Central Wavelength	1597.615 nm
Channel Spacing	100 GHz
Free Spectral Range (FSR)	1235 GHz
IO waveguide width	2.0 μm
IO waveguide pitch	5.5 μm
Array waveguide width	1.0 μm
Gap between array waveguides at FPR	0.6 μm
Array Acceptance Factor	2.0
Chirp factor	0.0

In Figure 4.12, it can be seen the results of the AWG 4x1 simulation in Aspic™. As referred in the previous chapter, in Aspic™, simulation after 1600 nm is not supported, so part of the filter response after this wavelength is not seen in the results. It can be seen that the lobes at the far right match the wavelengths of the channels of the Downstream. Likewise, the lobes corresponding to the channels of the Upstream also match the desired wavelengths. Between the Downstream and the Upstream there are the expected five repetitions due to the FSR. These repetitions are not an issue and they don't have to be suppressed, as in the AWG designs of the laser cavity, because at the input of this AWG 4x1 the channels are already well defined. In conclusion, this AWG works just like a multiplexer / demultiplexer and doesn't have to filter the signal.

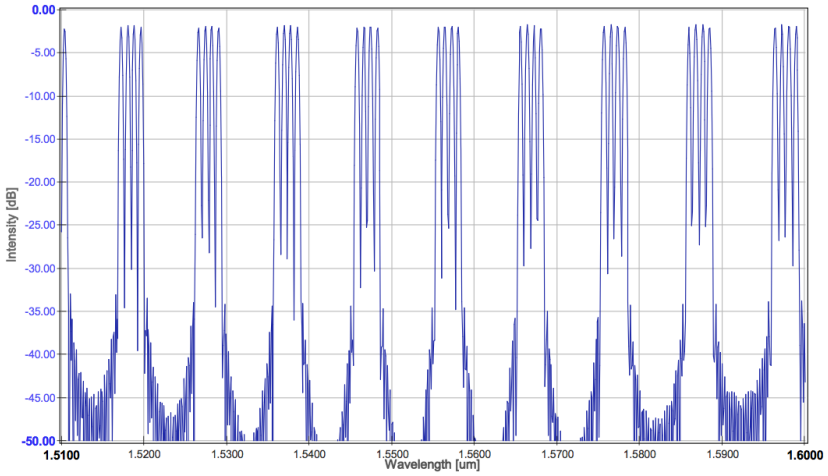


Figure 4.12: Response of the AWG 4x1 used as multiplexer and demultiplexer. Simulation in Aspic™.

4.4 Simulation of the Transmitter in VPItransmissionMaker™

With the laser cavity and the multiplexer already designed, the transmitter part of the transceiver can now be tested. Figure 4.13 shows the schematic of the transmitter used in the simulation in VPItransmissionMaker™. It can be observed that another block was used in this simulation, the Mach-Zehnder Modulator (MZM). The MZM is the device that modulates the input data that comes from the electrical signal. There is a MZM for each channel in order to be possible to transmit more than one channel in parallel to accomplish the TWDM.

The parameters of the MZM are not important for this simulation, because it is not done a time domain analysis. Furthermore, because of the lack of the PDK in the VPItransmissionMaker™, the model of the MZM from the foundry is not available for this simulation. However, some parameters that are in line with the state of the art of the MZM in InP were chosen, and Table 4.6 summarizes them.

Table 4.6: MZM Parameters used in VPItransmissionMaker™

Vπ DC	6 V
Vπ RF	6 V
Insertion Loss	2 dB
Device length	2 mm
Microwave Loss	0.005 dB/m/$\sqrt{Hz}$

Another addiction to this simulation is the incorporation in the test bench of the 4 SOAs that are between the MZMs and the multiplexer. These SOAs will provide more gain to the optical signal after the modulation and they can be used to tune the optical power needed for the different transmissions in the NG-PON2 standard. As will be explained in the receiver simulation section, these SOAs are also used to amplify the received signal when the transceiver is in receiver mode.

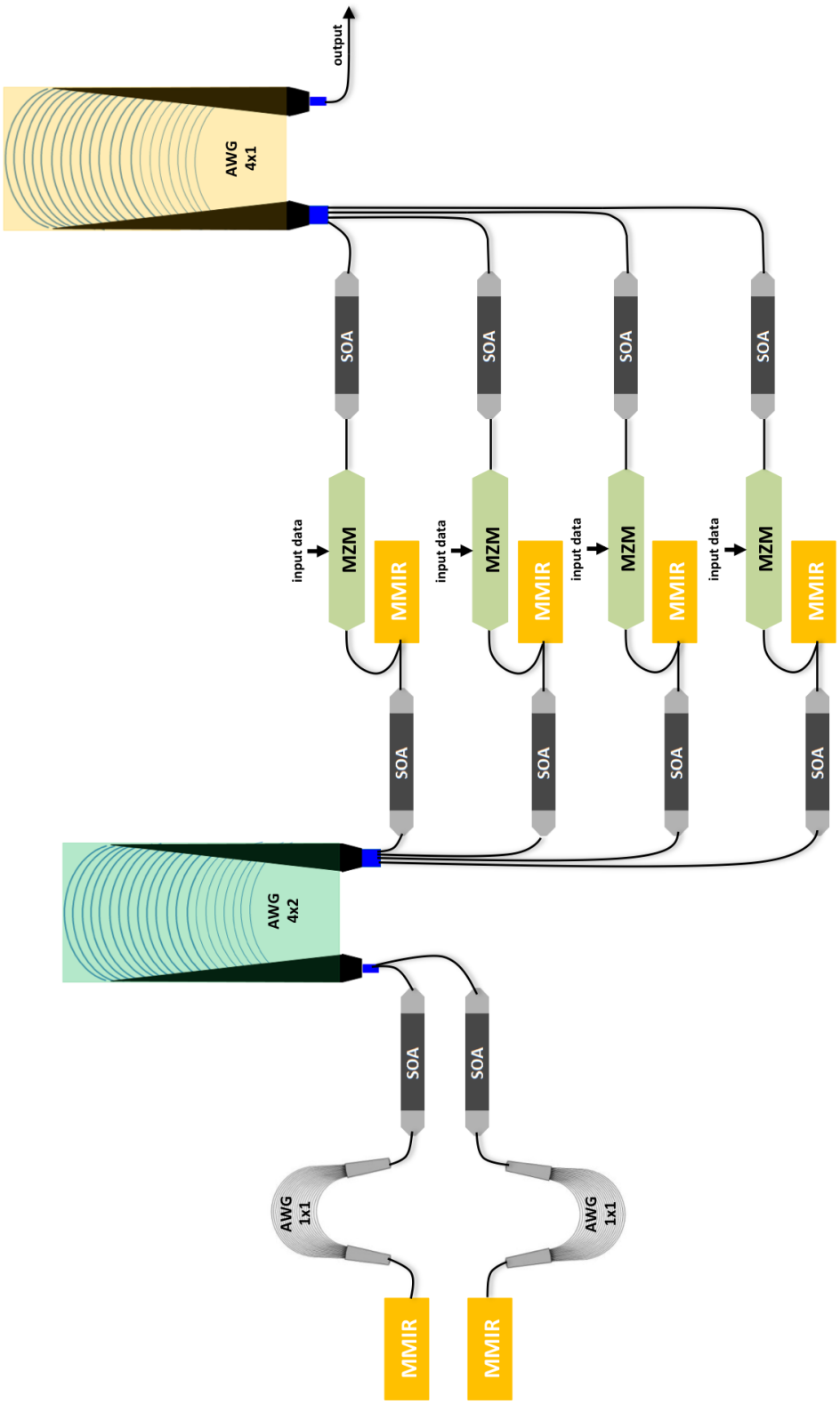


Figure 4.13: Block diagram of the transmitter simulation in VPItransmissionMaker™.

All the blocks were put together in the test bench and few simulations were performed. First, it was simulated a typical case of a transmission from the ONU, i.e. in the Upstream direction. In this case, the SOA corresponding to the Upstream was enabled and only one channel was activated from the four SOAs in parallel. Figure 4.14 displays the output spectrum of the transmitter after the MZMs. Then, a second simulation was realized, emulating the case of a transmission from the OLT. In this case, the SOA corresponding to the Downstream was enabled and all the SOAs that select the channels were activated. This represents a typical case in the Downstream transmission, as the OLT has to send data to several ONUs. Figure 4.15 presents the results of this simulation at the output of the MZMs.

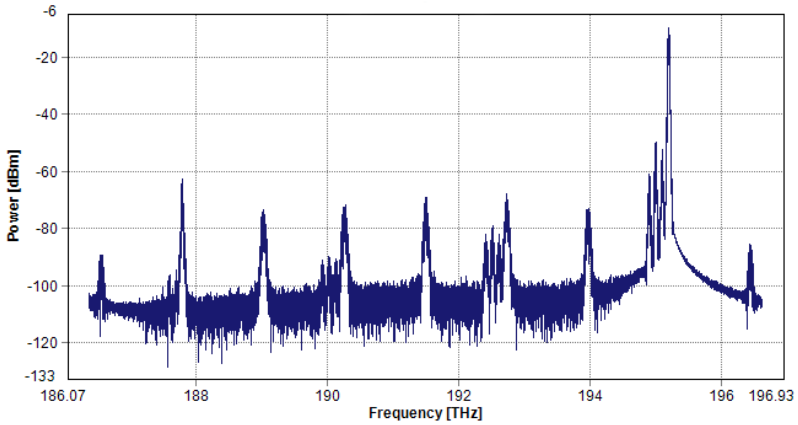


Figure 4.14: Simulation of the transmitter with ONU mode enabled (Upstream) with one channel activated in VPItransmissionMaker™. Optical power after the MZMs.

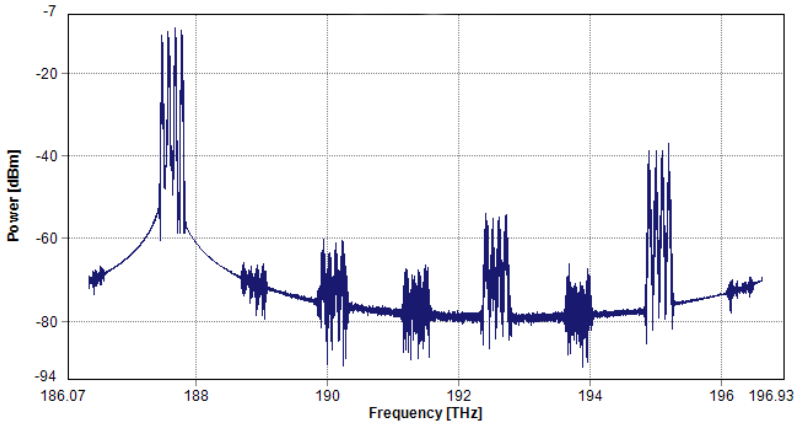


Figure 4.15: Simulation of the transmitter with OLT mode enabled (Downstream) with all channels activated in VPItransmissionMaker™. Optical power after the MZMs.

The total output power in both cases is approximately -10 dBm. Previously, in the simulation of the laser cavity, it was observed that there were small differences of power among the four channels transmitted simultaneously in the Downstream. The main contribution to this effect is the difference of the insertion loss in the channels of the AWGs of the laser cavity. This difference could be corrected with a slightly adjustment of the bias current of the SOAs, giving a little bit more gain to the side channels that have less output power. This correction was applied to the simulation here presented.

As referred before, the required transmission power defined by the NG-PON2 standard presented in Chapter 2 can be achieved using amplification of the additional SOAs presented before the multiplexer. Figure 4.16 and Figure 4.17 present the optical power after these SOAs and the output multiplexer for the same cases simulated before.

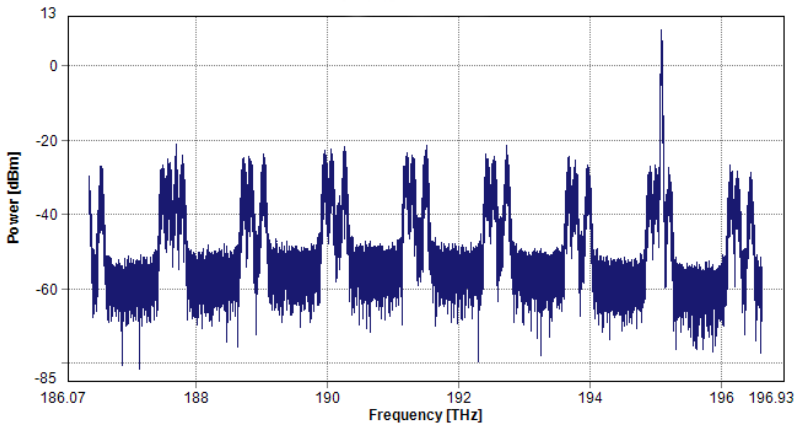


Figure 4.16: Simulation of the transmitter with ONU mode enabled (Upstream) with one channel activated in VPItransmissionMaker™. Optical output power of the transmitter.

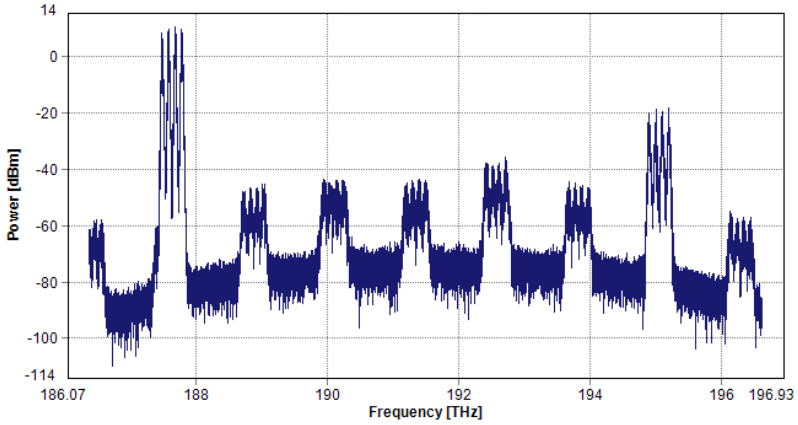


Figure 4.17: Simulation of the transmitter with OLT mode enabled (Downstream) with all channels activated in VPItransmissionMaker™. Optical output power of the transmitter.

The average power of the channels is now approximately +10 dBm. For NG-PON2 applications, the bias current of these SOAs can be changed slightly in order to put the required power defined by the standard at the output of the transmitter.

4.5 Simulation of the Receiver in VPItransmissionMaker™

After the demonstration of the transmitter, it was performed a simulation in VPItransmissionMaker™ to demonstrate the transceiver in receiver mode. Recalling Figure 4.1 with the complete block diagram of the transceiver, the received signal will come from the same unique optical interface presented in the PIC that is also used to transmit. So, for the received signal, the first building block that will encounter is the demultiplexer, the AWG 4x1. This block and the upcoming SOAs are components of the transceiver that are used bidirectionally. In the MMI device the paths are finally split and after this point different blocks are used for the transmitter and receiver. In the case of the receiver, the only upcoming block is the photodetector for each channel of the TWDM already demultiplexed.

Figure 4.18 shows the schematic of the receiver used in the simulation in VPItransmissionMaker™. New blocks were added to this schematic in comparison to the previous simulations. Firstly, the MMI device is now implemented in order to count with its contribution to the insertion loss. Again, because no model of the SMART Photonics PDK could be used, the parameters used in the incorporation of this building block in the simulation are shown in Table 4.7.

Table 4.7: MMI device Parameters used in VPItransmissionMaker™

Model Type	Self-imaging
Number of Left Ports	2
Number of Right Ports	1
MMI Type	Coupler
Width	3.5 μm
Effective Index	1.5
Group Index	4.2

Another building block added to the simulation, that is the key element for the receiver is the photodetector. The photodetector provided by SMART photonics is a PIN photodetector. No details are known about the characterization of this device, so general parameters were used in the simulation. Table 4.8 shows the parameters used in the PIN component in VPItransmissionMaker™.

Table 4.8: PIN photodetector Parameters used in VPItransmissionMaker™

Responsivity	1.0 A/W
Photodiode Model	PIN
Dark Current	0
Thermal Noise	10×10^{-12} A/$\sqrt{Hz}$

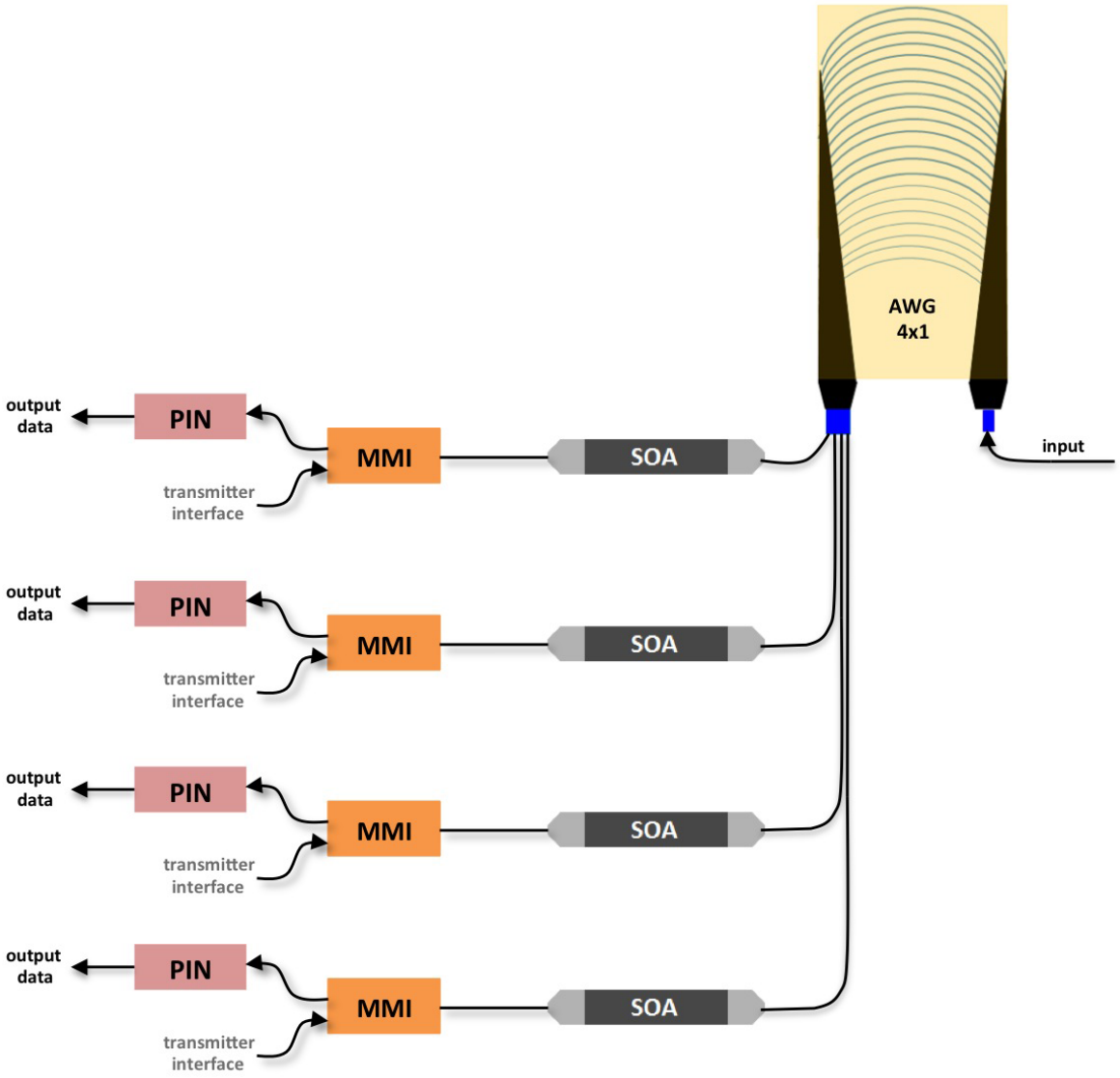


Figure 4.18: Block diagram of the receiver simulation in VPItransmissionMaker™.

Due to the lack of accuracy of not having the right models for the building blocks of the receiver, the main goal of this simulation in VPItransmissionMaker™ was to demonstrate the demultiplexing of the signal and the detection functionality of the photodetector. SOAs were not incorporated in the final simulation test bench, because when time-domain analysis are done, the output response of the amplifier is not completely settled, making difficult to perform the demonstration of the receiver. This behavior is due to the implementation of the model of the SOA presented before, that although it was successfully implemented and demonstrated in terms of frequency domain, in the time domain it was not possible to stabilize it. As the SOAs are missing in the receiver simulation, a link budget of the receiver path will be presented. Figure 4.19 presents the input signal (with approximately -10 dBm) used for the simulation to receive a Upstream signal with one channel enabled. In this case, the terminal that will receive a Upstream signal will be the OLT.

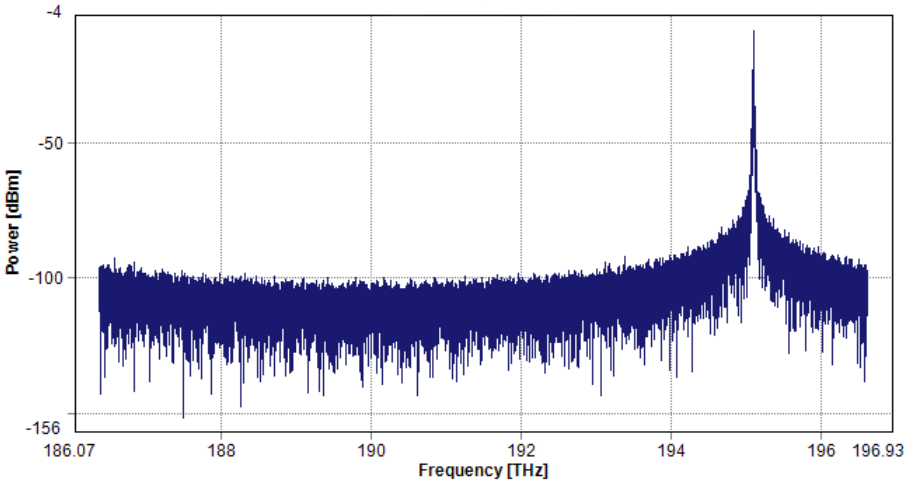


Figure 4.19: Input signal for the receiver in OLT mode (Upstream) with one channel activated. Simulation in VPItransmissionMaker™.

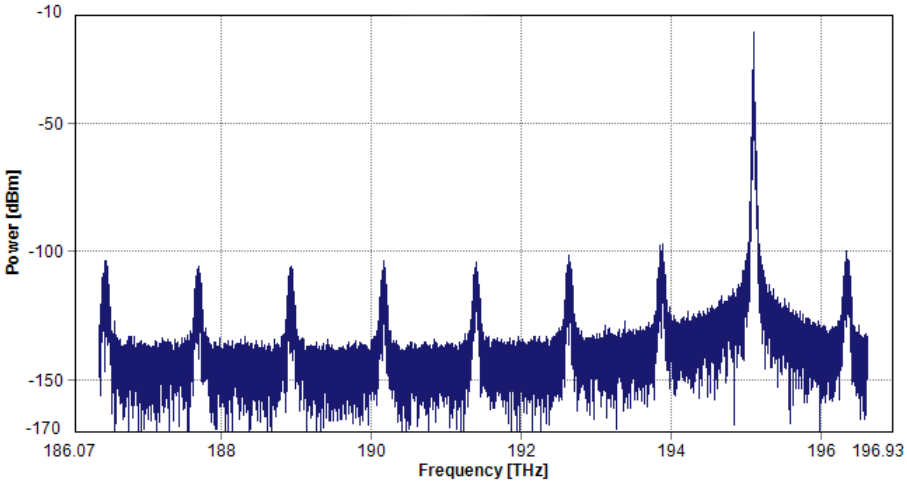


Figure 4.20: Optical power after the MMI device in the receiver in OLT mode (Upstream) with one channel activated. Simulation in VPItransmissionMaker™.

After the signal enters the receiver and goes through all the building blocks, it will suffer insertion loss from the AWG 4x1 and the MMI device. In Figure 4.20 it can be seen the signal power at the output of the MMI device before being detected by the PIN. The power at this point is -16 dBm, so the total insertion loss is estimated to be approximately 6 dB.

Finally, Figure 4.21 gives an example of the detected signal by the PIN photodiode.

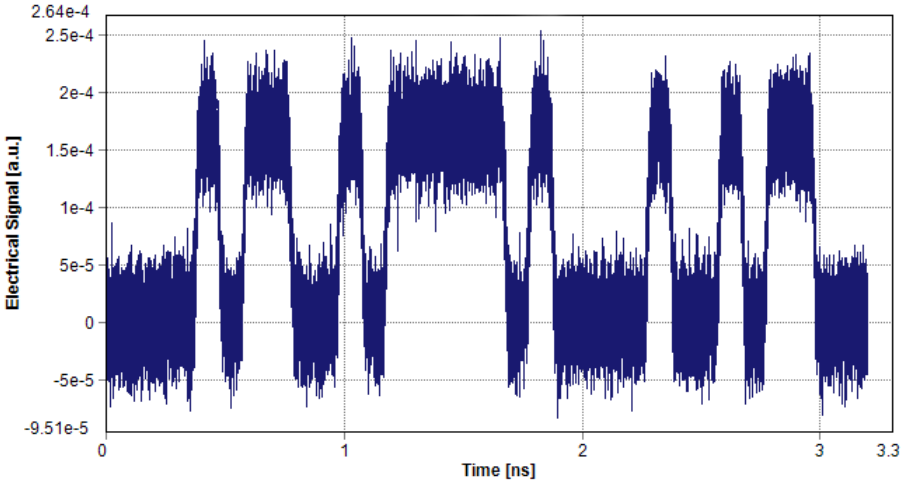


Figure 4.21: Detected signal by the PIN in the receiver in OLT mode (Upstream) with one channel activated. Simulation in VPItransmissionMaker™.

Similar simulations were performed for the Downstream transmission with more channels. It was also possible to demonstrate the functionality of the receiver in that mode. However, as the result of the detected data by the PIN photodiode gives similar outputs for these conditions, Figures are not shown here but they can be consulted in Appendix B.

4.5.1 Link Budget of the Receiver

As mentioned during the simulation analysis of the receiver, accurate simulation was not possible to be performed due to the lack of a model of the PIN photodetector and also due to the impossibility of having the SOAs working properly in the time-domain. Thus, in this section an estimation of the losses through the receiver path of the transceiver will be shown. This will work as reference for future simulations when the accurate models of the building blocks are available. The optical power received to be used as reference is the value that the NG-PON2 standard defines as minimum, i.e. the sensitivity of the receiver. The link budget is presented in Table 4.9.

Table 4.9: Link Budget of the Receiver

Minimum Received power (Sensitivity)	**-30 dBm**	Defined by NG-PON2
AWG 1x4 (Demux) Insertion Loss	-2 dB	Simulated in Aspic™
SOA Gain	+20 dB	Estimation
MMI device Maximum Insertion Loss	-4 dB	From the design manual
Optical power at the PIN input	**-16 dBm**	

With this calculation, one can conclude that the PIN photodetector has to have a sensitivity of at least -16 dBm in order to be able to demodulate the received signal. This value of power is consistent with the previous simulation. In Figure 4.20 it was shown the power after the MMI device, i.e. at the input of the PIN photodetector and it was also approximately -16 dBm.

4.6 Layout Implementation of the Transceiver

Previously, it was describing the transceiver architecture and performing demonstrations of the transmitter and receiver functionality. This section aims to present the layout implementation of the designed building blocks in the PIC. One important factor to take in account from the beginning is the total area available for the design. All cells provided by the foundry measure 4.6 x 4.0 mm^2. During the design procedure, it had to be taken in account the layout rules from the design manual, like minimum distances between waveguides, minimum separation between active blocks, etc.. The software used for the layout design was PhoeniX Software OptoDesigner that supports the PDK from SMART Photonics.

4.6.1 Layout implementation of the Laser Cavity

The section of the transceiver that occupies more area is without doubt the laser cavity. It was also the part of the architecture design that required more efforts to find a solution to enable the transceiver to be flexible and universal. Thus, the layout started from the laser cavity in order to locate all the components in strategic places to be possible to fit all the other building blocks inside the available area. The block diagram of the laser cavity was shown in Figure 4.10. Figure 4.22 displays the layout implementation of the laser cavity in OptoDesigner.

The bigger AWG on the top of the chip is the AWG 4x2. This AWG takes a lot of space, so the localization of it was critical. The 2 outputs of this AWG are connected to the SOAs that are located between the AWG 4x2 and the others (AWGs 1x1). These SOAs are the ones that work as switches to enable Downstream or Upstream transmission. Each AWG 1x1 has a reflector in one of the terminals, that is the MMIR device. From the other side of the AWG 4x2 through the waveguides to the bottom of the layout, the 4 inputs of the AWG 4x2 are connected to the 4 SOAs that enable which channels to transmit. These SOAs are then connected to the MMIR devices that reflect half power back to the cavity and split the other half to the rest of the transmitter. As mentioned in Chapter 4, the SOAs are 300 μm long and the parameters of the AWGs were obtained from the simulations in Aspic™.

The waveguides designed to connect the building blocks are deep waveguides. From the technology, there are two types of waveguides: shallow and deep waveguides. Shallow waveguides are preferred for long connections because they have low loss when compared to deep waveguides. However, shallow waveguides need a much larger bending radius, taking more space on the chip. For this reason, deep waveguides were chosen to be possible to do such tight curves shown in the layout. Most of the components have the possibility to have deep waveguides as their basis. Although, with SOAs it is only possible to use shallow waveguides, thus requiring transitions to the deep waveguides used for the connections. The foundry provides transition components that are optimized for this conversion to be smooth and to have low loss. This transition was used in the terminals of all SOAs.

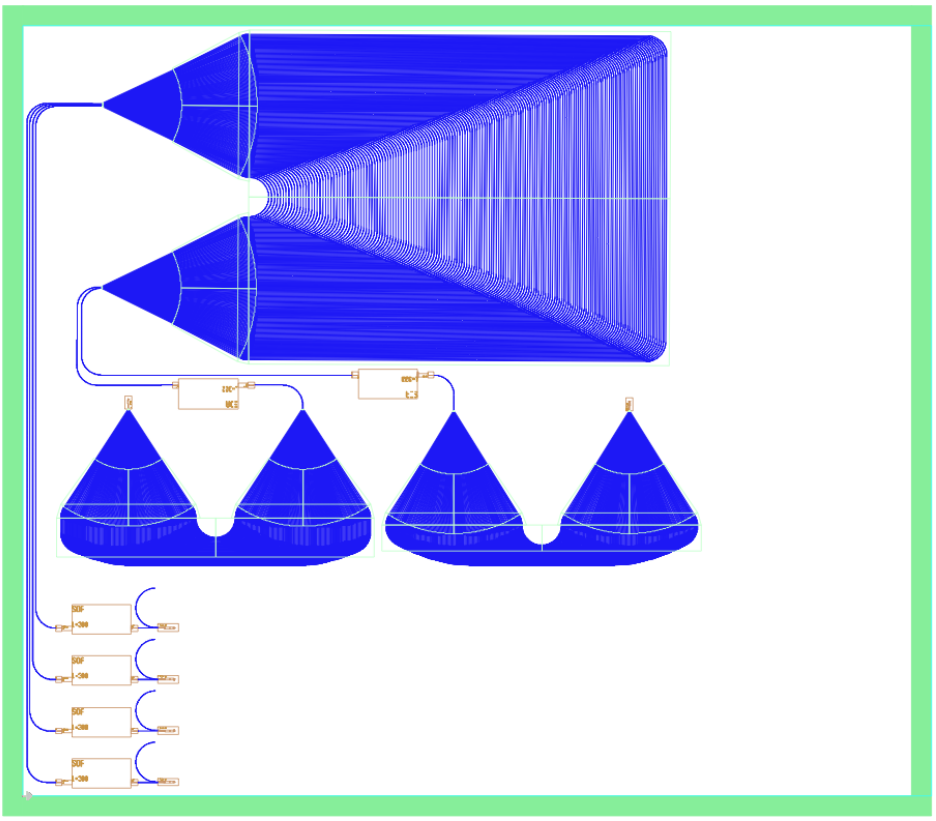


Figure 4.22: Layout implementation of the Laser Cavity in OptoDesigner.

4.6.2 Layout implementation of the Transmitter

The block diagram of the complete transmitter can be seen once again in Figure 4.13. Apart of the components that compose the Fabry-Pérot laser cavity, the transmitter also has 4 MZMs, 4 additional SOAs and the multiplexer (AWG 4x1). It has also the MMIs that split the signal between the transmitter and the receiver. Figure 4.23 displays the layout implementation of the transmitter in OptoDesigner.

The MZMs were positioned immediately after the MMIR reflectors (the output of the laser cavity). The MZMs are 2 mm long as stipulated in the parameters of the simulation in Chapter 4. They are composed by two phase shifters and one MMI device in each end. This complete structure of each MZM is automatically generated by the PDK tool. After the MZMs, it was inserted the MMI devices where the intersection between the transmitter and the receiver occurs. In the design of the MMI layout, it could be chosen between the usage of shallow or deep waveguides. Deep implementation was chosen so then no additional transitions were necessary. The following SOAs located on the bottom right of the layout are the additional amplifiers to provide the required output power. Finally, the multiplexer was positioned in the remaining layout area, with the output close to the edge of the cell. The output of the AWG 4x1 is connected to the optical interface to the exterior. This interface is a waveguide with a angled facet. It was used a angled facet, because the facet reflections are reduced when the light hits the chip facet at an angle.

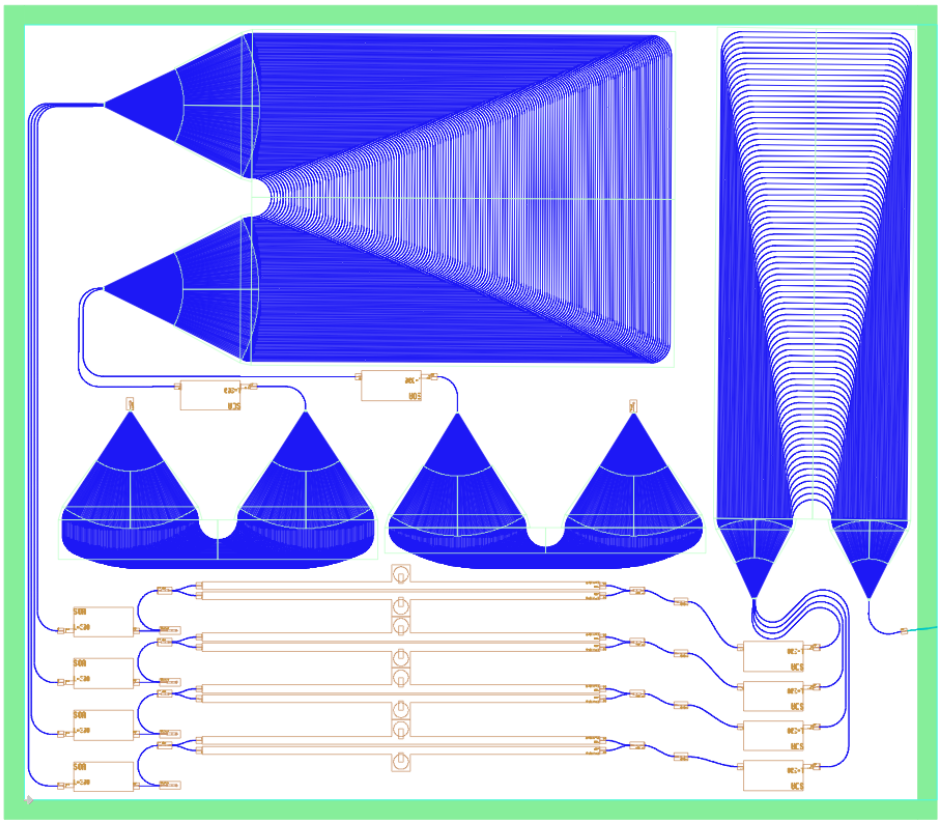


Figure 4.23: Layout implementation of the Transmitter in OptoDesigner.

4.6.3 Layout implementation of the Receiver

Most of the building blocks that are part of the receiver structure of the transceiver were already implemented on the layout of the transmitter (the demultiplexer, the SOAs and the MMI devices). The component still missing and the most important one for the receiver is the PIN photodetector. The complete block diagram can be checked once again in Figure 4.18. Figure 4.24 shows the layout of the transceiver, now with the receiver too. The only addiction in comparison to Figure 4.23 is now the inclusion of the 4 PIN photodetectors. They are connected to the MMI devices in the bottom right of the layout.

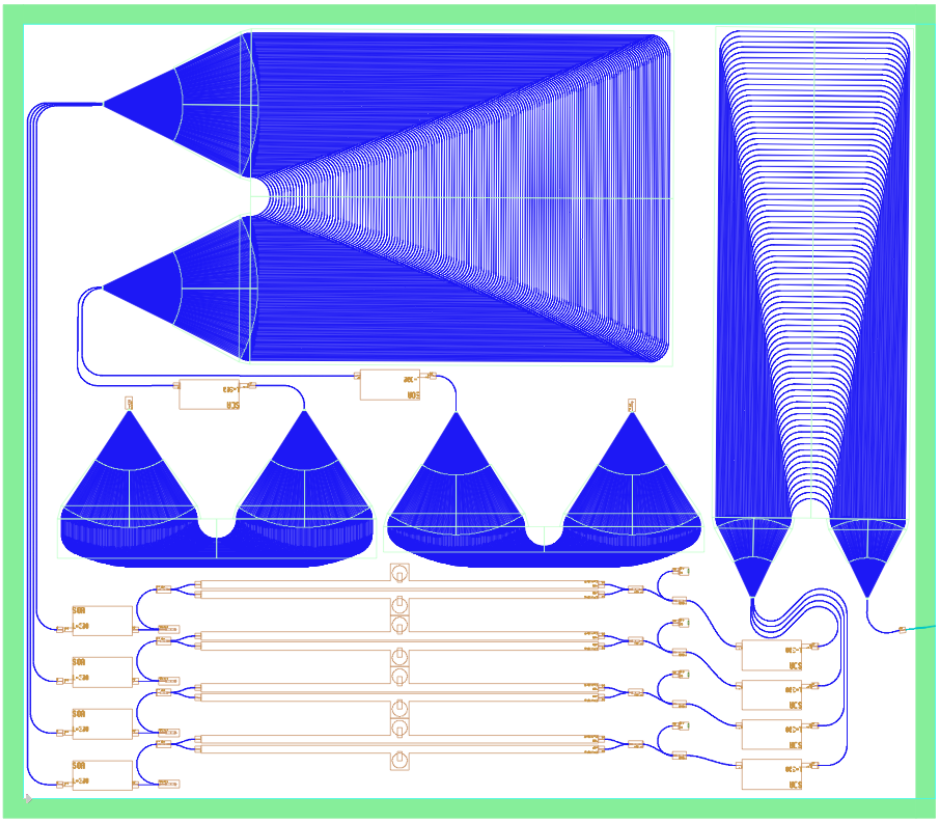


Figure 4.24: Layout implementation of the Transmitter and the Receiver in OptoDesigner.

4.6.4 Final Layout of the Transceiver

With the layout of the transmitter and the receiver blocks completed with all the interconnections, the pads for the electrical connections were then implemented. In Figure 4.25 it is shown the full layout of the transceiver implemented in OptoDesigner.

Several pads had to be included in the PIC. Firstly, the pads for the bias current of the SOAs. These are DC pads. There are 6 on the left side and 4 on the right side. The 6 pads of the left side are related to the SOAs inside the laser cavity - the two on the top to select Downstream / Upstream and the other four to select the channels. The 4 SOAs of the right side are the ones to provide bias to the amplifiers used by the transmitter and by the receiver.

On the bottom of the chip are located the RF pads. There are RF pads for the transmitter and for the receiver. The transmitter needs 8 RF pads, 2 for each MZM. Due to the space limitation, four pads were positioned more to the left and the other four were positioned more to the right. The two connections for each MZM were designed with the aim for the signals to have the same distance, as the input signal will be differential and requires symmetry. However, full equalization was not possible to be designed due to the lack of space for the signals routing. This happens mainly with the MZM on the bottom. The other MZMs have practically equal connections to the two arms.

The remaining RF pads are the ones used for the receiver. They are the 4 pads at the far right on the bottom of the chip. Each pad was connected to the corresponding PIN photodiode.

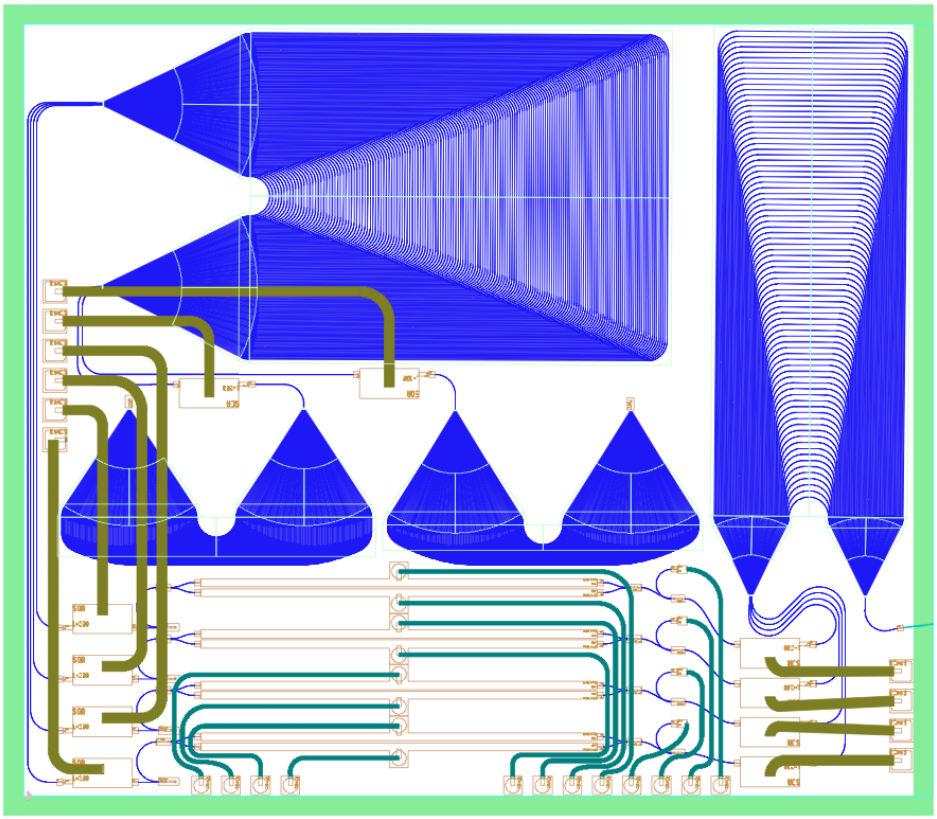


Figure 4.25: Full Layout implementation of the Transceiver in OptoDesigner.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

This dissertation had the goal to implement a Photonic Integrated Circuit (PIC) for Next Generation Passive Optical Network Phase 2 (NG-PON2), intended to be a universal transceiver. The PIC had to be able to be used as an Optical Line Terminal (OLT) or an Optical Network Unit (ONU) and in both cases as transmitter and receiver.

After an introduction that explains the need to find a solution to overcome the limits of the capacity of the telecommunications networks due to the increase of users, who require more bandwidth and higher speeds, it was proceeded to a study about the only technology capable to overcome this problem, the optical communications.

Firstly, it was presented some basic concepts about the Passive Optical Network (PON) architecture, and the currently standard in development, NG-PON2. Thereafter, it was explored the current trend in optical technologies, the PICs. Due to their characteristics of integration, they allow speed enhancement keeping the power consumption as low as possible and the reliability is increased. Additionally, it was referred the different materials used for the development and production of PICs and which are the existing foundries. From the chosen process for the PIC development in this dissertation, SMART Photonics, it was shown the design flow and some fundamental requirements for the development of the PIC. Finally, it was presented theory about the building blocks that were utilized in the design of the transceiver.

In order to implement the transceiver, it was exposed different architectures for the laser cavity of the transceiver to fulfill the outlined requirements. Each architecture was designed and simulated, using Aspic™, and then some remarks were done about the advantages and the disadvantages. In the end, a final architecture was chosen for the PIC development, performing a key block, an AWG 4x2.

Then, the transceiver was designed and simulated block by block. First, the Fabry-Pérot cavity was demonstrated in Aspic™. After the laser cavity, a model of the SOA had to be implemented in VPItransmissionMaker™. At this stage, the full functionality of the laser cavity could be proven, emitting all channels of the Downstream and the Upstream. Thereafter, the last components of the transmitter were added in VPItransmissionMaker™ and the complete transmitter could be simulated. The transmitter was tested in OLT mode and ONU mode. Finally, the photodetectors and the MMI devices were added and the transceiver in receiver mode was shown too.

Lastly, the layout of the PIC was implemented based on the parameters of the simulations performed before.

Overall, it can be concluded that the requirements for the PIC development for NG-PON2 were achieved in this dissertation and the PIC can be implemented as a universal transceiver. It is expected that this work will be a useful contribution to the technology development in optical communications.

5.2 Future Work

As future work, the following points are suggested to be explored:

- During this work it was successfully implemented the layout of the projected building blocks that compose the universal transceiver. These components fit inside the available area provided by the foundry. However, one suggestion for future work could be the reduction of the dimensions of the AWGs. These are the components that occupy most of the PIC area. Any improvement in their dimensions, keeping the required performance, would be very beneficial in terms of costs or even to use the remaining area for additional blocks.

- The architecture developed in this work doesn't include the possibility to process coherent signals, since this was not a requirement according to the NG-PON2 standard. Nonetheless, optical communications will develop for higher order modulations, using IQ transmissions. Taking this into account, a future version of this transceiver most probably would need an adaption for this type of transmissions. According to the previous point, if it would be possible to have more area available, additional blocks related to the IQ transmission and reception could be added. Thus, the transceiver would be also prepared for modulations like QPSK.

- In Chapter 4, simulations of the complete transceiver were performed. It was specified which components had models close to the parameters provided by the foundry. One important building block to have an accurate model was the SOA. The model used for this component was developed previously and in most of the simulations it was sufficient. However, in case of the receiver when time-domain simulations were run, it was observed inconsistent results that were related to the fact that the SOAs were not settling. For this reason, the receiver was simulated without the inclusion of the amplifiers and a link budget was presented to address this exclusion. Hence, it would valuable in future developments to have a model of the SOA that could perform accurate time-domain simulations, and not only in frequency domain.

Appendixes

Appendix A

VPItransmissionMaker™ Simulation Schematics

In this Appendix it is presented pictures of the schematics used in VPItransmissionMaker™ for the transceiver simulations. Figure A.1 shows the schematics of the transmitter for simulation in VPItransmissionMaker™. Figure A.2 shows the schematics of the receiver for simulation in VPItransmissionMaker™.

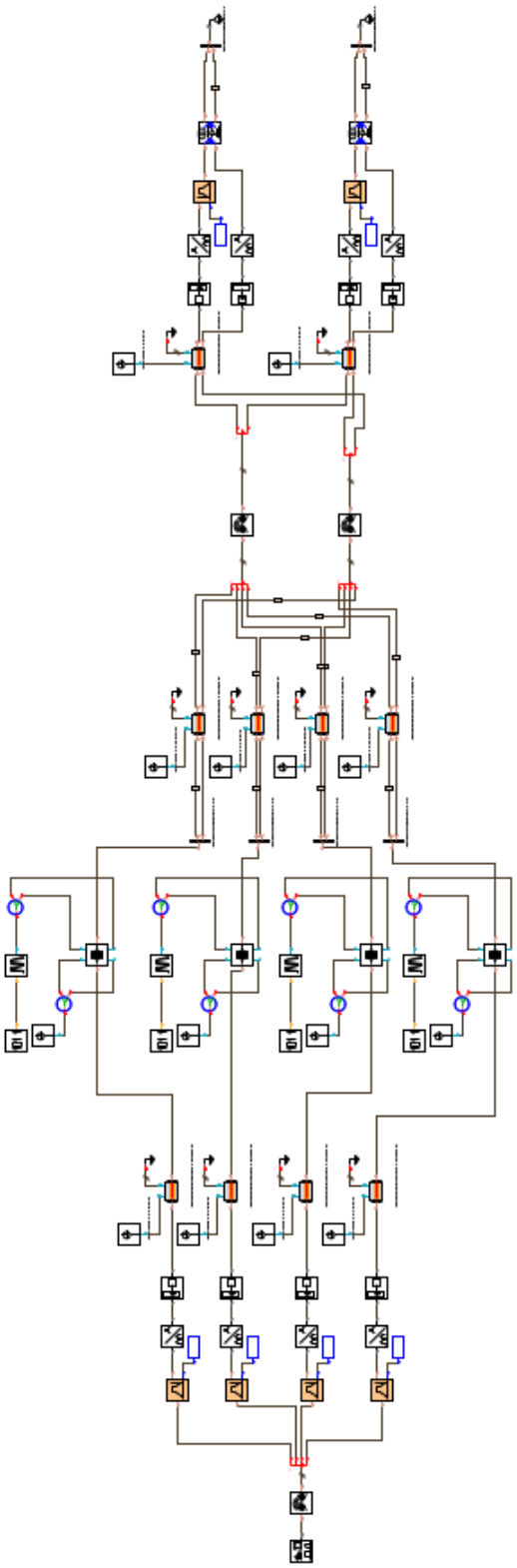


Figure A.1: Schematics of the Transmitter for simulation in VPItransmissionMaker™.

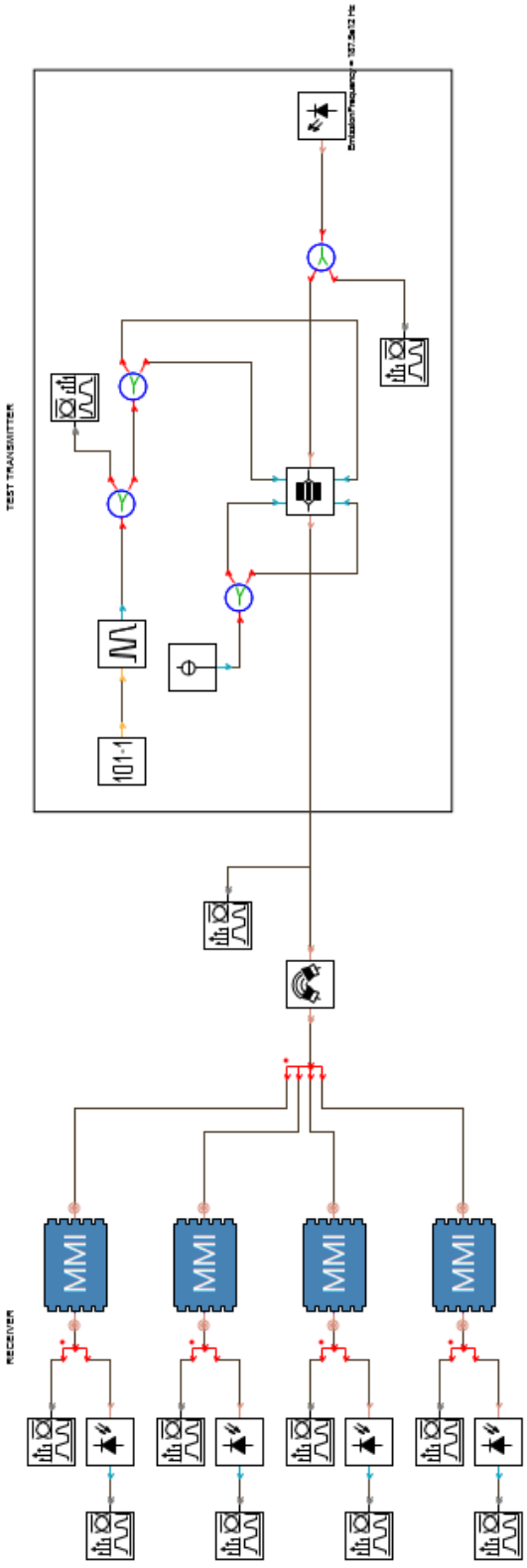


Figure A.2: Schematics of the Receiver for simulation in VPItransmissionMaker™.

Appendix B

Simulation of the Receiver in Downstream mode

In section 4.5, the receiver was simulated showing a demonstration for Upstream transmissions. Similar experiments were performed for Downstream, however they were not included in the same section due to not being sufficient relevant for the receiver demonstration.

In this appendix, the results of the receiver simulation in Downstream mode are provided. In Figures B.1 to B.4, it can be seen the signal power at the output of the MMI device before being detected by the PIN for the 4 channels in a Downstream transmission.

Finally, Figure B.5 gives the output detected signal by the PIN photodiode. The result is the same for the 4 channels.

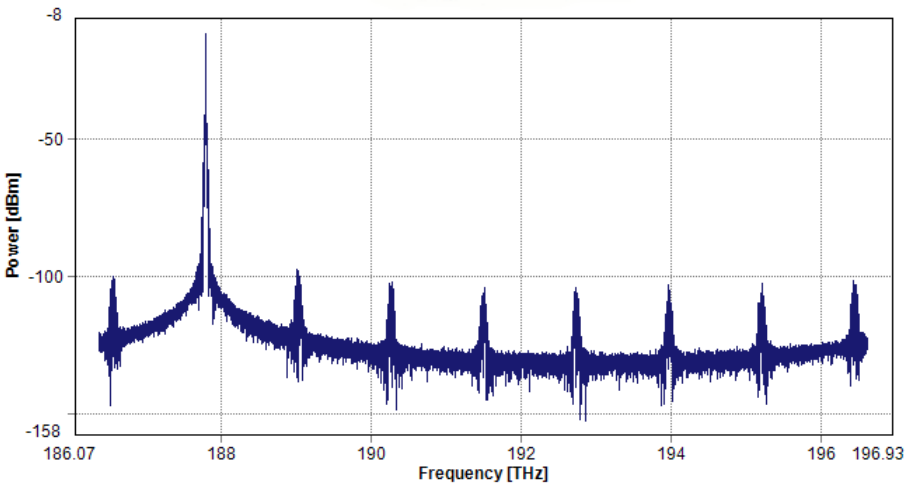


Figure B.1: Optical power after the MMI device in the receiver in ONU mode (Downstream), first channel. Simulation in VPItransmissionMaker™.

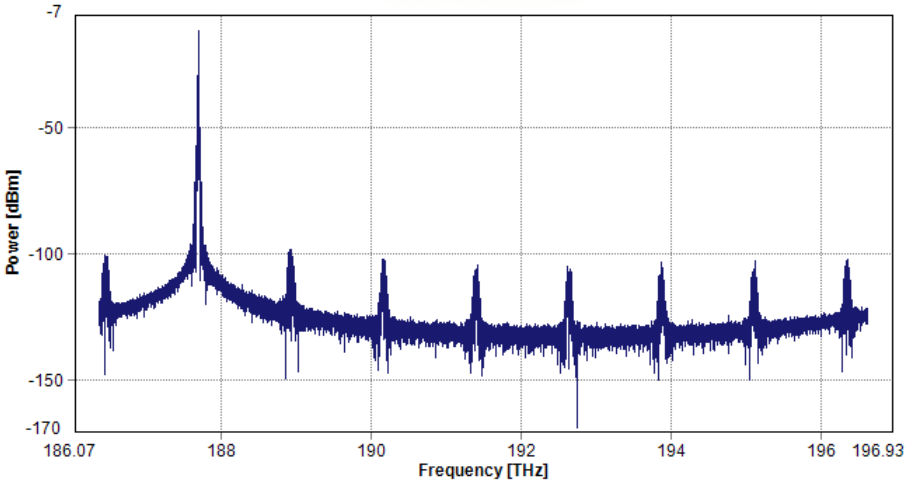


Figure B.2: Optical power after the MMI device in the receiver in ONU mode (Downstream), second channel. Simulation in VPItransmissionMaker™.

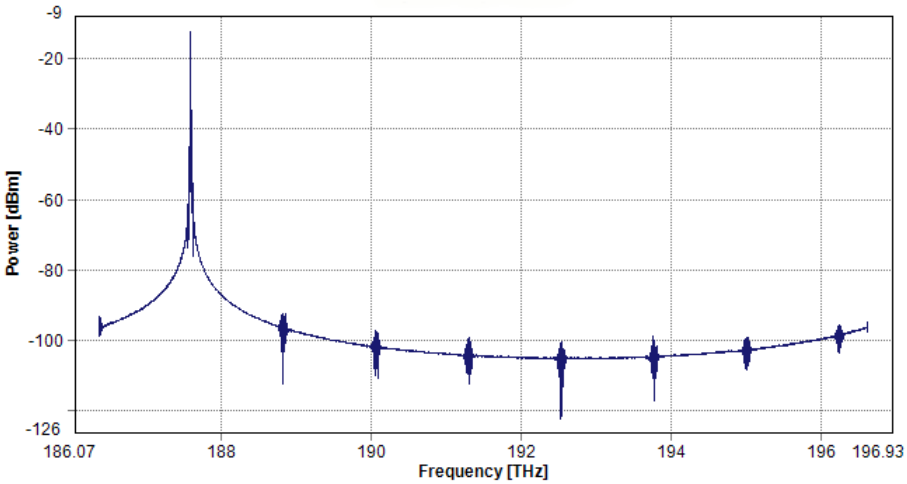


Figure B.3: Optical power after the MMI device in the receiver in ONU mode (Downstream), third channel. Simulation in VPItransmissionMaker™.

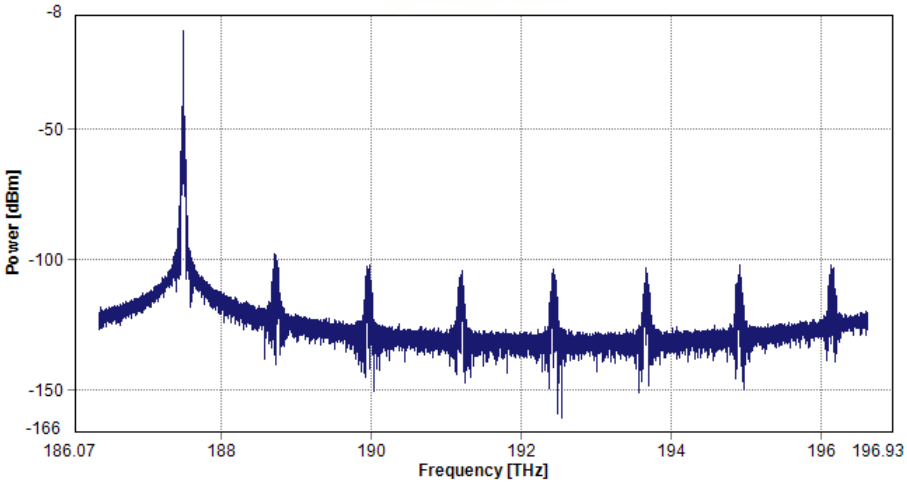


Figure B.4: Optical power after the MMI device in the receiver in ONU mode (Downstream), fourth channel. Simulation in VPItransmissionMaker™.

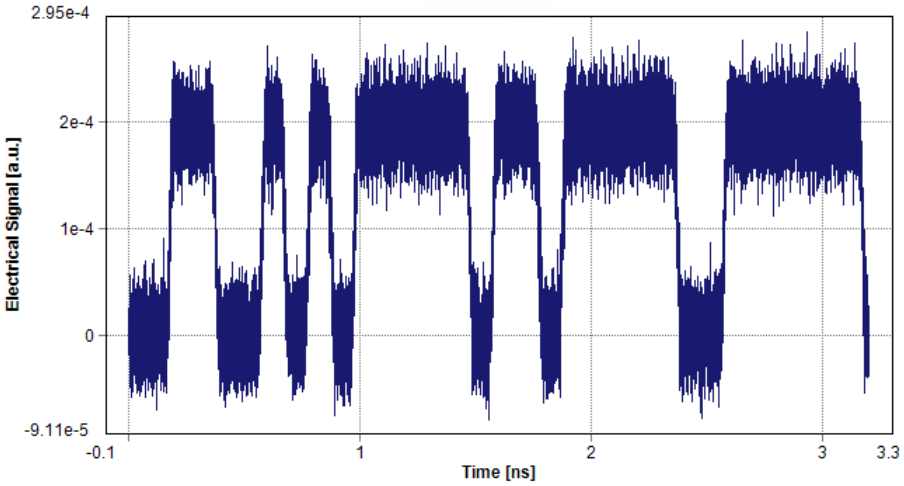


Figure B.5: Detected signal by the PIN in the receiver in ONU mode (Downstream). Simulation in VPItransmissionMaker™.

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